ANRITSU

MP1632A

The Anritsu MP1632A is a high-performance Digital Data Analyzer and Bit Error Rate Tester (BERT) operating from 50 MHz to 3.2 GHz. Designed for testing high-speed digital transmission systems, it uniquely integrates a Pulse Pattern Generator (transmitter) and an Error Detector (receiver) into a single compact unit. Utilizing a user-friendly Windows-based graphical interface on a large LCD, the MP1632A supports comprehensive PRBS, consecutive zero, and programmable pattern generation, along with specialized burst-signal measurements for optical loop testing and eye margin analysis.

SPECIFICATIONS

General

Display	Large Color TFT LCD with GUI

Physical

Power Supply	100 to 120 V AC / 200 to 240 V AC, 47.5 to 63 Hz, ≤ 450 VA
Dimensions (W×H×D)	426 mm × 221.5 mm × 451 mm mm
Weight	25 kg kg

Frequency & Clock Generation

Operating Frequency Range	50 MHz to 3.2 GHz
Frequency Resolution	1 kHz steps

Pattern Generator

PRBS Test Patterns	2^n - 1 (n = 7, 9, 11, 15, 20, 23, 31)
Programmable Pattern Length	2 to 8,388,608 bits
Generator Clock/Data Output Amplitude	0.25 Vp-p to 2.0 Vp-p (10 mV steps)
Generator Clock/Data Output Offset Range	-2.0 V to +2.0 V (10 mV steps)
Generator Clock/Data Rise and Fall Time	≤ 90 ps (20% to 80%)

Error Detector & Measurements

Eye Margin Measurement Error Rate Range	1 x 10^-n (n = 3 to 9)
Burst Signal Measurement	Supported (generation and measurement for optical loop tests)
Eye Diagram Measurement	Supported (useful for quality evaluation of input waveforms)

Controller & System

Internal Operating System	Windows OS

System Configuration

System Architecture	Integrated Pulse Pattern Generator (transmitter) and Error Detector (receiver) in a single unit
Far-end Measurement Capability	Configurable as two separate units (transmitting and receiving)

Error Detector

Detector Data Input Voltage Range	0.05 Vp-p to 2.0 Vp-p
Detector Clock Input Voltage Range	0.1 Vp-p to 2.0 Vp-p

Reference Clock

Internal Reference Clock Frequency	10 MHz
External Reference Input Frequency	10 MHz

Generator

Clock-Data Delay Range	±1000 ps
Clock-Data Delay Resolution	1 ps
Output Impedance	50 Ω
Output Connector Type	SMA female

Detector

Input Impedance	50 Ω
Input Connector Type	SMA female
Auto-Search Functions	Threshold, Phase

Error Insertion

Error Insertion Modes	Single, Rate, External
Internal Error Insertion Rate	1E-3 to 1E-9

TECHNOLOGY

Bit Error Rate Testing (BERT)

APPLICATIONS

Evaluating high-speed digital transmission circuits, optical loop testing, and eye diagram quality verification.