ANRITSU

MP1800A

The Anritsu MP1800A Signal Quality Analyzer is a highly expandable, plug-in, modular bit error rate tester (BERT) platform designed for signal integrity analysis. It supports multi-channel bit error rate (BER) testing from 0.1 Gbit/s up to 32.1 Gbit/s (and up to 64.2 Gbit/s with external MUX/DEMUX), making it ideal for characterizing optical transceivers (AOC, CFP, CXP, QSFP+), backplanes, and high-speed chips.

SPECIFICATIONS

General

Interfaces	LAN (10/100/1000 Base-T), GPIB, USB 2.0 (Host & Device), VGA, Reference Clock I/O
Display	12.1-inch SVGA color TFT LCD with touch screen (800 x 600 resolution)
Warm-up Time	30 minutes
Cooling	Forced air by cooling fan
Module Hot-swapping	Not supported

Physical

Power Supply	100 V AC to 120 V AC / 200 V AC to 240 V AC, 47.5 Hz to 63 Hz, ≤ 650 VA
Operating Temperature	5 to 40 °C
Dimensions (W×H×D)	426 x 221.5 x 451 mm
Weight	15 kg

Mainframe & System Architecture

Chassis Slot Capacity	6 slots for plug-in modules
Operating Bit Rate Range (Standard)	0.1 Gbit/s to 32.1 Gbit/s
Operating Bit Rate Range (with External MUX/DEMUX)	Up to 64.2 Gbit/s
Multi-channel Synchronization	Up to 8 channels at 32 Gbit/s within a single mainframe
Maximum Scaled Configuration	Up to 32 channels (32G x 32ch) utilizing multi-mainframe control

Pulse Pattern Generator (PPG) Module Specs

PPG Channels per Module	1ch, 2ch, or 4ch options
PPG Maximum Output Amplitude	Up to 3.5 Vp-p (supports EA/EML modulator evaluation)
PPG Output Rise/Fall Time	12 ps (typical, 20% to 80%)
PPG Intrinsic Jitter	8 ps p-p (typical)
PPG De-emphasis Integration	4-tap emphasis up to 32.1 Gbit/s (with external MP1825B)

Error Detector (ED) Module Specs

ED Channels per Module	1ch, 2ch, or 4ch options
ED Minimum Input Sensitivity	10 mV (typical)
ED Clock Recovery	Embedded clock recovery supported
ED Equalizer Integration	Passive Linear Equalizers supported for improved eye opening

Jitter & Noise Tolerance Testing

Jitter Modulation Types	SJ (Sinusoidal Jitter), RJ (Random Jitter), BUJ (Bounded Uncorrelated Jitter), SSC (Spread Spectrum Clock), Dual-Tone SJ, HPJ (Half Period Jitter)
Sinusoidal Jitter (SJ) Maximum Amplitude	Up to 2000 UI at low frequency
Sinusoidal Jitter (SJ) High Frequency Range	Up to 1 UI at 250 MHz

Pattern & Sequence Generator Capabilities

PAM Pattern Support	32.1 Gbaud PAM4 generation and accurate PAM4 BER measurement
Burst Pattern Generation	Automated generation of burst data and auxiliary signal timings (E-PON, G-PON, 10GE-PON)

Software & Measurement Analysis

Signal Analysis Modes	Bathtub Measurement (TJ, DJ, RJ), Eye Diagram, Eye Margin, and Burst Measurement
Application Testing Support	Crosstalk evaluation, skew tolerance, and EDFA loop circuit testing

Environmental

Storage Temperature Range	-20 °C to +60 °C
Operating Humidity Range	35% to 85% RH (non-condensing)
Acoustic Noise	≤ 60 dBA

Reference Clock

Reference Clock Input Frequency	10 MHz
Reference Clock Input Level	0.5 Vp-p to 2.0 Vp-p
Reference Clock Output Frequency	10 MHz
Reference Clock Output Level	≥ 1.0 Vp-p (into 50 Ω)

System & Software

Operating System	Windows XP Professional / Windows 7 (configuration dependent)

Pattern Generation (PPG)

PPG PRBS Pattern Lengths	2^7-1, 2^9-1, 2^11-1, 2^15-1, 2^20-1, 2^23-1, 2^31-1

Error Detection (ED)

ED PRBS Pattern Lengths	2^7-1, 2^9-1, 2^11-1, 2^15-1, 2^20-1, 2^23-1, 2^31-1

Clock Synthesizer

Synthesizer Frequency Resolution	1 kHz (with internal synthesizer module)

Connectivity & Control

Remote Control Command Language	SCPI

Compliance

Safety Standard Compliance	EN 61010-1
EMC Standard Compliance	EN 61326-1, EN 55011

TECHNOLOGY

Bit Error Rate Testing (BERT)

APPLICATIONS

Signal Integrity Analysis, Transceiver Testing (100G/400G), Jitter Tolerance Testing