KEYSIGHT TECHNOLOGIES (AGILENT HP)

16557D

The Keysight (Agilent/HP) 16557D is a 68-channel logic analyzer state and timing analysis module designed for the HP 16500C and Agilent 16700 series mainframes. Featuring a 135 MHz (up to 140 MHz) state speed and 500 MHz timing analysis, the 16557D offers a deep 2M sample acquisition memory to help isolate complex, time-correlated bugs across high-speed digital systems and buses.

SPECIFICATIONS

General

Display	None (requires mainframe display)

Physical

Power Supply	Powered via mainframe backplane
Operating Temperature	0 °C to +55 °C °C

Acquisition and Channels

Number of Channels	68 channels per module
Maximum State Clock Speed	135 MHz
Maximum Timing Sample Rate	500 MHz
State/Timing Correlation	Simultaneous, fully time-correlated state analysis on some channels and timing analysis on the rest
Multi-Module Expansion	68 to 340 channels (up to 5 modules cascaded on a single time base and data trigger)

Memory and Record Length

Standard Memory Depth	2 M samples per channel

Mainframe Compatibility

Compatible Mainframes	HP 16500C, Agilent 16700, 16700A, 16700B, 16702A, 16702B
Backplane Slot Width Requirements	1 slot

Input Signal Characteristics

Input Impedance	100 kΩ parallel with approximately 8 pF at probe tip
Minimum Input Voltage Swing	500 mV peak-to-peak
Threshold Voltage Range	-6.0 V to +6.0 V
Threshold Voltage Resolution	50 mV
Maximum Input Voltage	±40 V peak

Triggering and Sequencing

Trigger Sequence Levels	12 levels
Pattern Recognizers	10
Range Recognizers	2
Edge/Transition Terms	2
Timer Resources	2

Timing Analysis

Conventional Timing Sample Rate	500 MHz (half-channel) / 250 MHz (full-channel)
Transitional Timing Sample Rate	125 MHz
Glitch Timing Sample Rate	125 MHz (half-channel)

State Analysis

State Clocks / Qualifiers	4 clocks
Minimum State Eye Width	4.0 ns
Setup and Hold Window	3.5 ns, adjustable in 100 ps increments

Memory

Maximum Memory Depth (Half-Channel Mode)	4,194,304 samples

Accessories

Compatible Probe Cables	Keysight 10474A, 10483A

Channels & Inputs

Number of Pods	4
Channels per Pod	17 (16 data, 1 clock/data)

TECHNOLOGY

Logic Analyzer Module

APPLICATIONS

Digital design debugging, bus analysis, and time-correlated state/timing measurements

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