KEYSIGHT TECHNOLOGIES (AGILENT HP)

# 1661C

The HP / Agilent / Keysight 1661C is a high-performance benchtop logic analyzer designed for debugging and validating complex digital systems. It provides 102 state and timing channels, a state speed of up to 100 MHz, and a timing speed of up to 500 MHz in half-channel mode. Equipped with built-in HP-IB and RS-232C interfaces as well as a 3.5-inch floppy disk drive, it is a robust and classic troubleshooting tool for legacy and embedded hardware designs.

## SPECIFICATIONS

### General

| | |
|---|---|
| Interfaces | HP-IB (GPIB), RS-232C |
| Display | 9-inch monochrome CRT (640 × 350 resolution) |

### Physical

| | |
|---|---|
| Power Supply | 115/230 V AC (-22% to +10%), 48-66 Hz, 200 W maximum |
| Operating Temperature | 0 to 55 °C °C |
| Dimensions (W×H×D) | 425 mm × 188 mm × 432 mm mm |
| Weight | 11.8 kg kg |

### Performance

| | |
|---|---|
| Number of State and Timing Channels | 102 channels |
| Maximum State Analysis Rate | 100 MHz |
| Maximum Conventional Timing Rate (Full Channel) | 250 MHz |
| Maximum Conventional Timing Rate (Half Channel) | 500 MHz |
| Maximum Transitional Timing Rate (Full Channel) | 125 MHz |
| Maximum Transitional Timing Rate (Half Channel) | 250 MHz |
| Memory Depth per Channel (Full Channel) | 4,096 samples |
| Memory Depth per Channel (Half Channel) | 8,192 samples |
| Trigger Sequence Levels | 12 levels |
| Trigger Pattern Recognizers | 10 |
| Trigger Range Recognizers | 2 |
| Trigger Edge/Glitch Recognizers | 2 |
| Channel-to-Channel Skew | < 2 ns (typical) |

### System Architecture

| | |
|---|---|
| Storage Type | 3.5-inch Floppy Disk Drive (FDD), 1.44 MB DOS format |

### Inputs & Outputs

| | |
|---|---|
| Probe Input Resistance | 100 kΩ |
| Probe Input Capacitance | approximately 8 pF |
| External Trigger Input | BNC, TTL compatible |
| External Trigger Output | BNC, TTL compatible |

### Environmental

| | |
|---|---|
| Maximum Operating Altitude | 4,600 m (15,000 ft) |
| Storage Temperature Range | -40 to +75 °C |

### Input Probes

| | |
|---|---|
| Threshold Range | -6.0 V to +6.0 V in 50 mV increments |
| Threshold Accuracy | ±(100 mV + 3% of threshold setting) |
| Minimum Input Voltage Swing | 500 mV peak-to-peak |
| Maximum Input Voltage | ±40 V peak |

### State Analysis

| | |
|---|---|
| Minimum Clock Pulse Width | 3.5 ns |
| Setup/Hold Time | 3.5/0 ns or 0/3.5 ns (user selectable, single clock, single edge) |
| Number of State Clocks | 6 |

### Timing Analysis

| | |
|---|---|
| Minimum Glitch Width | 3.5 ns |

### Data Storage

| | |
|---|---|
| File Formats | MS-DOS, LIF |
| Floppy Drive Format Support | DOS (1.44 MB, 720 KB) / LIF (1.44 MB, 610 KB) |

### Tagging & Measurements

| | |
|---|---|
| Time Tag Resolution | 8 ns or 0.1% (whichever is greater) |
| Maximum Time Tag Duration | 34.4 seconds |
| State Tag Counter Size | 24-bit |
| Maximum State Tag Count | 1.67 × 10^7 |

### Probing

| | |
|---|---|
| Input Dynamic Range | ±10 V |
| Preset Thresholds | TTL, CMOS, ECL |

### Power Requirements

| | |
|---|---|
| AC Input Voltage Range | 90 V to 264 V AC (auto-ranging) |
| AC Line Frequency | 48 Hz to 66 Hz |
| Maximum Power Consumption | 200 W |

## TECHNOLOGY

Logic Analyzer

## APPLICATIONS

Digital system design, hardware troubleshooting, embedded systems testing

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