

## KEYSIGHT TECHNOLOGIES (AGILENT HP)

# 1662C

The Keysight 1662C (originally HP/Agilent 1662C) is a benchtop logic analyzer offering 68 channels for comprehensive state and timing analysis. Designed with a built-in 9-inch color CRT display, the 1662C provides timing speeds up to 500 MHz and a state speed up to 100 MHz, making it a reliable tool for hardware integration and digital troubleshooting.

## SPECIFICATIONS

### General

|            |                                                                                    |
|------------|------------------------------------------------------------------------------------|
| Interfaces | HP-IB (GPIB), RS-232C, Centronics Parallel Printer Port, PS/2-style keyboard/mouse |
| Display    | 9-inch color CRT, 640 x 480 resolution                                             |

### Physical

|                       |                                                     |
|-----------------------|-----------------------------------------------------|
| Power Supply          | 115/230 V AC auto-ranging, 48-66 Hz, 200 VA maximum |
| Operating Temperature | 0 °C to +50 °C °C                                   |
| Dimensions (W×H×D)    | 358 mm x 190 mm x 445 mm mm                         |
| Weight                | 11.8 kg                                             |

### Measurement Capabilities

|                           |    |
|---------------------------|----|
| State and Timing Channels | 68 |
|---------------------------|----|

### State Analysis

|                                 |                                      |
|---------------------------------|--------------------------------------|
| Maximum State Analysis Rate     | 100 MHz                              |
| Minimum State Clock Pulse Width | 3.5 ns                               |
| State Setup / Hold Time         | 3.5 ns / 0 ns                        |
| Number of State Clocks          | 4                                    |
| Number of Clock Qualifiers      | 4                                    |
| Time Tagging Resolution         | 8 ns or 0.01% (whichever is greater) |
| Minimum State Clock Period      | 10 ns                                |

### Timing Analysis

|                                                 |         |
|-------------------------------------------------|---------|
| Maximum Conventional Timing Rate (Full Channel) | 250 MHz |
| Maximum Conventional Timing Rate (Half Channel) | 500 MHz |
| Maximum Transitional Timing Rate (Full Channel) | 125 MHz |
| Maximum Transitional Timing Rate (Half Channel) | 250 MHz |
| Minimum Glitch Width Detected                   | 3.5 ns  |

## Memory & Acquisition

|                             |                  |
|-----------------------------|------------------|
| Memory Depth (Full Channel) | 4 KB per channel |
| Memory Depth (Half Channel) | 8 KB per channel |

## Storage

|                               |                                            |
|-------------------------------|--------------------------------------------|
| Floppy Disk Drive             | 3.5-inch 1.44 MB double-sided high-density |
| Supported Floppy Disk Formats | MS-DOS, LIF                                |

## Triggering

|                            |                             |
|----------------------------|-----------------------------|
| Trigger Sequence Levels    | 12 levels                   |
| Pattern Recognizers        | 10 pattern recognizers      |
| Range Recognizers          | 2 range recognizers         |
| Edge/Glitch Recognizers    | 2 edge/glitch recognizers   |
| Trigger Occurrence Counter | Up to 1,048,575 occurrences |
| Number of Timers           | 2                           |

## Environmental

|                          |                                   |
|--------------------------|-----------------------------------|
| Operating Altitude Limit | 4,600 m (15,000 ft)               |
| Relative Humidity Range  | Up to 90% non-condensing at 40 °C |

## Input Characteristics

|                             |                                                      |
|-----------------------------|------------------------------------------------------|
| Input Impedance             | 100 k $\Omega$ $\pm$ 2% in parallel with $\sim$ 8 pF |
| Maximum Input Voltage       | $\pm$ 40 V peak                                      |
| Minimum Input Voltage Swing | 500 mV peak-to-peak                                  |
| Threshold Setting Range     | -6.0 V to +6.0 V in 50 mV steps                      |
| Threshold Accuracy          | $\pm$ (100 mV + 3% of setting)                       |
| Input Dynamic Range         | $\pm$ 10 V                                           |

## Architecture

|                |   |
|----------------|---|
| Number of Pods | 4 |
|----------------|---|

## Inputs & Outputs

|                         |                     |
|-------------------------|---------------------|
| External Trigger Input  | BNC, TTL compatible |
| External Trigger Output | BNC, TTL compatible |

## Interfaces

|                               |      |
|-------------------------------|------|
| Programmable Control Language | SCPI |
|-------------------------------|------|

## TECHNOLOGY

Logic Analysis

## APPLICATIONS

Digital circuit troubleshooting, embedded system debugging, and bus analysis

