KEYSIGHT TECHNOLOGIES (AGILENT HP)

16700A

The Agilent (Keysight) 16700A is a 5-slot modular logic analysis system mainframe in the 16700 Series. It provides a scalable chassis with an integrated web server for remote operation and time-correlated measurements across domains, from analog signals to source code. The frame requires an external monitor and accepts two additional accessory slots for emulation modules, and can be expanded to 10 measurement slots with the 16701A expansion frame.

SPECIFICATIONS

General

Display	External monitor required (no internal display)

System Architecture and Mainframe

Mainframe type	Modular logic analysis system mainframe
Series	16700 Series
Measurement module slots	5
Accessory/emulation slots	2
Expansion frame model	16701A expansion frame (compatible)
Total measurement slots with 16701A	10 (when connected to 16701A)

Display and User Interface

User interaction	Keyboard and mouse supported
Internal display	None (external display required)
User interface	Graphical user interface for setup and operation
External display requirement	External monitor required (system has no internal display)

Acquisition Performance — State Analysis

Maximum State Clock Rate	Module-dependent (per installed state acquisition module)
State Clocking Modes	Module-dependent
Source-Synchronous Clock Support	Module-dependent
DDR/Double-Transition Capture	Module-dependent
Setup Time Measurement Range	Module-dependent
Setup Time Resolution	Module-dependent
Hold Time Measurement Range	Module-dependent
Hold Time Resolution	Module-dependent
State Skew (Channel-to-Channel)	Module-dependent
State Timing Accuracy	Module-dependent
State Acquisition Memory Depth per Channel	Module-dependent
Store Qualification Modes	Module-dependent
Transitional Storage (State)	Module-dependent
Memory Segmentation (State)	Module-dependent
Pre-Trigger/Post-Trigger Allocation (State)	Module-dependent
Minimum Arm-to-Trigger Latency (State)	Module-dependent
Re-Arm Time (State)	Module-dependent
State Time Stamp Resolution	Module-dependent
State Time Stamp Accuracy	Module-dependent

Acquisition Performance — Timing Analysis

Timing Sample Rate	Module-dependent
Timing Resolution	Module-dependent
Minimum Detectable Glitch Width	Module-dependent
Timing Acquisition Memory Depth per Channel	Module-dependent
Timing Zoom/Eye Resolution	Module-dependent
Channel-to-Channel Skew (Timing)	Module-dependent
Acquisition Jitter (Timing)	Module-dependent
Minimum Pulse Width	Module-dependent
Edge Timing Accuracy	Module-dependent
Transitional Storage (Timing)	Module-dependent
Memory Segmentation (Timing)	Module-dependent
Pre-Trigger/Post-Trigger Allocation (Timing)	Module-dependent
Acquisition Dead Time (Timing)	Module-dependent
Burst/Interleaved Timing Modes	Module-dependent

Trigger System

Sequential Trigger States	Module-dependent
Trigger Resources (Timers/Counters)	Module-dependent
Pattern/Edge/Level Trigger	Module-dependent
Glitch/Transition Trigger	Module-dependent
Setup/Hold Violation Trigger	Module-dependent
Range/Window Trigger	Module-dependent
Duration/Timeout Trigger	Module-dependent
Occurrence/Counter Trigger	Module-dependent
Trigger Qualification (Edge/Level)	Module-dependent
Trigger Across Modules	Module-dependent (coordinated operation when supported by installed modules)
Prestore/Poststore Control	Module-dependent
Trigger Position in Memory	Module-dependent
Arming Modes	Module-dependent
Trigger Holdoff	Module-dependent
Event Markers	Module-dependent

Timebase and Correlation

Time correlation across modules	Supported by system architecture; specifics per module
Timebase/clock characteristics	Module-dependent (specified by installed modules)
Intermodule time alignment	Module-dependent
Skew calibration (intermodule)	Module-dependent
Marker delta time resolution	Module-dependent

Input and Probe Characteristics

Number of channels per module	Module-dependent
Channels per pod	Module-dependent
Pod count per module	Module-dependent
Probe interface type	Module-dependent
Input voltage threshold range	Module-dependent
Threshold resolution	Module-dependent
Threshold accuracy	Module-dependent
Per-channel/per-pod threshold setting	Module-dependent
Input hysteresis	Module-dependent
Input impedance	Module-dependent
Input capacitance	Module-dependent
Maximum safe input voltage	Module-dependent
Common-mode range	Module-dependent
Single-ended/differential support	Module-dependent
Termination options	Module-dependent
Pod-to-pod skew	Module-dependent
Ground leads per pod	Module-dependent
Flying lead set compatibility	Module-dependent
Target connector interface	Module-dependent
Auto-threshold detection	Module-dependent
Threshold calibration	Module-dependent
Logic family support	Module-dependent
Clock qualifier probe support	Module-dependent
Probe power from target	Module-dependent
ESD protection	Module-dependent

Pattern Generator (optional)

Channels (pattern generator)	Module-dependent
Maximum output rate (pattern generator)	Module-dependent
Data/clock timing resolution (pattern generator)	Module-dependent
Output voltage levels (pattern generator)	Module-dependent
Output drive strength (pattern generator)	Module-dependent
Edge placement resolution (pattern generator)	Module-dependent
Per-channel skew adjustment (pattern generator)	Module-dependent
Pattern memory depth	Module-dependent
Pattern sequencer states	Module-dependent
Loops/branches/waits	Module-dependent
Marker outputs (pattern generator)	Module-dependent
External clock input (pattern generator)	Module-dependent
Output connector type (pattern generator)	Module-dependent
Intermodule synchronization (pattern generator)	Module-dependent

Mixed-Signal / Oscilloscope Modules (optional)

Maximum analog sample rate	Module-dependent
Vertical range (analog)	Module-dependent
Vertical resolution (analog)	Module-dependent
Analog memory depth	Module-dependent
Analog trigger types	Module-dependent
Time correlation with digital channels	Supported across installed modules; specifications module-dependent
Analog input impedance	Module-dependent
Analog probe compatibility	Module-dependent

Measurement and Analysis Features

Waveform display	Supported
State listing display	Supported
Bus/group definitions	Supported
Inverse assembler support	Supported (software-dependent)
Search and filter functions	Supported
Save/Recall setups	Supported

Ordering Information

Base model ordering code	16700A