

KEYSIGHT TECHNOLOGIES (AGILENT HP)

16720A

The Keysight (Agilent) 16720A is a high-performance 48-channel digital pattern generator module designed for use with the 16900 and 16700 Series modular logic analysis systems. Capable of a maximum stimulus clock rate of up to 300 MHz and memory depths of up to 16 M vectors, it is an essential tool for digital design verification, functional debugging, and stress testing under both standard and infrequently encountered conditions.

SPECIFICATIONS

General

Interfaces	Front-panel pod connectors, External trigger input, External clock input, Mainframe backplane interface
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Physical

Power Supply	Supplied by mainframe backplane
Operating Temperature	0 to 50 °C °C

Timing and Frequency Specifications

Maximum Stimulus Clock (Half Channel)	300 MHz
Maximum Stimulus Clock (Full Channel)	150 MHz

Pattern Generation

Memory Depth (Half Channel)	16 M vectors
Memory Depth (Full Channel)	8 M vectors
Maximum Vector Width (Half Channel)	120 bits
Maximum Vector Width (Full Channel)	240 bits
Pattern Entry Tools	Multiple number bases and pattern fills
Vector Entry Simplification	INIT block, user-defined macros, and loops

Channel and Configuration Options

Number of Channels per Module	48
Maximum Cascaded Channels	240 (by connecting up to 5 modules)
Clock Pod Requirement	At least one clock pod for each module used as a master (ordered separately)
Data Pod Requirement	At least one data pod for every 8 output channels (ordered separately)

System, Control and Interfaces

File Conversion Support	SynaptiCAD tools convert .VCD files into .PGB files directly
Compatible Mainframes	Agilent 16700 Series modular logic analyzers

Trigger and Synchronization

Trigger Synchronization	Wait for External Event
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Clocking

Internal Clock Period Range	3.3 ns to 20.48 μ s
External Clock Input Frequency	DC to 300 MHz (half-channel), DC to 150 MHz (full-channel)

Sequencer

Sequencer Instructions	Wait, Repeat, Loop, Call, Return, Halt
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Environmental

Storage Temperature	-40 °C to +75 °C
Operating Humidity	Up to 95% RH (non-condensing) at +40 °C

Power Requirements (from Mainframe)

+5 V Current Draw	1.5 A
-5.2 V Current Draw	4.0 A
-2 V Current Draw	1.5 A
+12 V Current Draw	0.1 A

Hardware Configuration

Slot Width	1 slot
Number of Pod Connectors	6

Timing and Clocking

Clock Out Delay Range	0 ns to 11 ns
Clock Out Delay Resolution	100 ps

Sequencer Specifications

Maximum Sequencer Instructions	4000
Maximum Loop Count	1,048,575
Maximum Nesting Levels	4

Compatible Pods

Supported Logic Pods	10461A TTL/CMOS, 10462A 3-State TTL/CMOS, 10464A ECL (Terminated), 10465A PECL, 10466A LVDS, 10483A 3-State TTL/CMOS
Supported Clock Pods	10460A TTL/CMOS, 10463A ECL, 10468A PECL, 10469A LVDS

TECHNOLOGY

Digital Pattern Generation

APPLICATIONS

Functional verification, debugging, and stress testing of digital designs

