KEYSIGHT TECHNOLOGIES (AGILENT HP)

16910A

The Keysight (formerly Agilent) 16910A is a 102-channel logic analyzer module designed for 16900 Series logic analysis systems. It features 4 GHz high-speed timing zoom with a dedicated 64K memory, conventional timing analysis up to 1 GHz, and state analysis clock rates up to 450 MHz. This flexible module supports multiple upgrade options for memory depth (up to 32M) and state speed, allowing it to scale with evolving digital design and debug requirements.

SPECIFICATIONS

General

Interfaces	Three 90-pin cable connectors for probe connections
Display	None (uses mainframe display)

Physical

Power Supply	Power supplied by 16900 series mainframe backplane
Operating Temperature	0 to 50 °C °C
Weight	1.6 kg kg
Slot Width	1 slot

Acquisition and Channel Specifications

Number of Channels	102
High-Speed Timing Mode (Zoom Timing) Sample Rate	4 GHz (250 ps)
High-Speed Timing Mode Memory Depth	64K
Maximum Timing Sample Rate - Full Channel	500 MHz
Maximum Timing Sample Rate - Half Channel	1 GHz
Maximum Timing Sample Rate - Transitional Timing	500 MHz
Selectable Memory Depths	256K, 1M, 4M, 16M, or 32M (option dependent)

State Analysis Characteristics

Maximum State Clock Rate (Base - Option 250)	250 MHz
Maximum State Clock Rate (Upgraded - Option 500)	450 MHz
Maximum State Data Rate (Base - Option 250)	250 Mb/s
Maximum State Data Rate (Upgraded - Option 500)	500 Mb/s
State Threshold Range	-3.0 V to 5.0 V
State Threshold Setting Resolution	10 mV
Eye Finder / Eye Scan Support	Supported (automatically adjusts setup and hold)

Mainframe and System Integration

Compatible Mainframes	Keysight / Agilent 16900 Series

Memory and State Speed Upgrade Options

Option 256	Acquisition memory depth of 256K (included in base configuration)
Option 001	Increase acquisition memory depth to 1M at purchase
Option 004	Increase acquisition memory depth to 4M at purchase
Option 016	Increase acquisition memory depth to 16M at purchase
Option 032	Increase acquisition memory depth to 32M at purchase
Option 250	Maximum state speed of 250 MHz (included in base configuration)
Option 500	Increase maximum state speed to 450 MHz at purchase

Input Channels

State Clocks	4 clocks (J, K, L, M)
Minimum Signal Swing	300 mV p-p
Maximum Input Voltage	±40 V peak

Connectivity

Compatible Probes	Keysight 90-pin logic analyzer probes (e.g., E5381A, E5382A, E5390A)

Triggering

Trigger Sequence Levels	16
Pattern Detectors	16
Range Detectors	4
Edge/Glitch Detectors	2
Timers/Counters	2

Environmental

Storage Temperature Range	-40 °C to +75 °C
Operating Altitude	Up to 3,000 m (10,000 ft)
Non-operating Altitude	Up to 15,300 m (50,000 ft)

Performance

State Mode Minimum Eye Width (Option 500)	1.5 ns
State Mode Minimum Eye Width (Option 250)	2.0 ns
Setup/Hold Adjustment Resolution	100 ps steps

Compliance

Safety Compliance	IEC 61010-1, EN 61010-1, CSA C22.2 No. 61010-1, UL 61010-1
EMC Compliance	IEC 61326-1, EN 61326-1, ICES-001, AS/NZS CISPR 11

TECHNOLOGY

Logic Analysis

APPLICATIONS

Digital hardware debugging, bus analysis, state and timing measurements