KEYSIGHT TECHNOLOGIES (AGILENT HP)

3784A

The Keysight (Agilent/HP) 3784A is a high-performance Bit Error Rate (BER) and jitter test set designed for manufacturing, commissioning, and maintenance of telecommunication networks and equipment operating at CEPT interface rates (704 kb/s, 2, 8, and 34 Mb/s). Featuring a built-in synthesized clock source, TTL/ECL binary interfaces for versatile BER testing from 1 kb/s to 50 Mb/s, and options for 64 kb/s codirectional and jitter interfaces, it delivers robust automated testing of jitter tolerance, jitter transfer functions, and comprehensive error analysis.

SPECIFICATIONS

General

Display	CRT display

Physical

Power Supply	100 / 120 / 220 / 240 V AC, 48 to 66 Hz
Operating Temperature	0 to 55 °C °C
Dimensions (W×H×D)	425 mm × 188 mm × 530 mm mm
Weight	19 kg kg

Receiver and Transmitter Interfaces

Supported CEPT Bit Rates	704 kb/s, 2 Mb/s (2.048 Mb/s), 8 Mb/s (8.448 Mb/s)
General-Purpose BER Rate Range	1 kb/s to 50 Mb/s
Binary Interfaces	TTL, ECL
Optional Interfaces	64 kb/s codirectional interface (Option 002)

Clocking and Synchronization

Clock Source Type	Internal synthesized clock source

Error Insertion and Measurement

Error Analysis Parameters	Error count, error ratio, error and error-free intervals (seconds or deciseconds), % unavailability, % errored seconds, % severely errored seconds, % degraded minutes
Measurement Mode	Simultaneous measurement of all error analysis parameters

Jitter and Wander Measurements

Jitter Measurement Parameters	Peak-to-peak amplitude, jitter hit count, jitter hit and hit-free intervals (seconds or deciseconds)
Automated Jitter Measurements	Fully automated jitter tolerance and transfer function measurements (up to and beyond CCITT limits)
Through-Data Jitter Modulation	Supported (adds jitter to a fully-framed test signal passing through)
Jitter and Error Correlation	Correlation of jitter hits with error bursts

Framing and Overhead Analysis

In-Service Monitoring	Line code error detection for monitoring in-service performance

System Control and Connectivity

Results Logging	Unattended long-term measurement logging to external printer
Ease-of-Use Features	Measurement presets, automatic receiver set-up, pass/fail thresholds

Receiver Specifications

Receiver Input Impedance	75 Ω unbalanced (BNC), 120 Ω balanced (Siemens 3-pin)

Transmitter Specifications

Transmitter Output Impedance	75 Ω unbalanced (BNC), 120 Ω balanced (Siemens 3-pin)
Line Coding	HDB3, AMI
Internal Clock Accuracy	±10 ppm

Test Patterns

PRBS Test Patterns	2^9-1, 2^11-1, 2^15-1, 2^20-1, 2^23-1

Jitter Generator

Jitter Modulation Sources	Internal synthesizer, external input

Transmitter

Transmitter Clock Offset	±50 ppm in 1 ppm steps

Receiver

Receiver Input Modes	Terminate, Monitor, Protected Monitor

Transmitter / Error Generation

Error Insertion Rates	Single, 1E-3, 1E-4, 1E-5, 1E-6, 1E-7
Error Insertion Types	Bit, Code (bipolar violation)

Compliance

Standards Compliance	ITU-T G.703, G.821, G.823, O.171

Options

Option 001	Adds 704 kb/s operating rate

TECHNOLOGY

Bit Error Rate & Jitter Testing

APPLICATIONS

Commissioning, manufacturing, and maintenance of CEPT telecom network equipment

Generated by SpecAtlasHub (specatlashub.com). Specifications are compiled from available sources and are subject to change — verify critical values against the manufacturer before purchase.