KEYSIGHT TECHNOLOGIES (AGILENT HP)

86108A

The Keysight (formerly Agilent) 86108A Precision Waveform Analyzer is a double-wide plug-in module designed for the 86100C Infiniium DCA-J mainframe. It delivers outstanding accuracy for testing high-speed digital communications signals, featuring an integrated clock recovery system, an ultra-low residual jitter timebase, and high-bandwidth electrical channels in a single integrated unit. This setup enables simple, single-connection 'triggerless' measurements on serial data streams up to 14.2 Gb/s.

SPECIFICATIONS

General

Interfaces	Mainframe backplane (host mainframe provides GPIB, LAN, and USB)
Display	None (utilizes host mainframe display)

Physical

Power Supply	Powered directly by the host mainframe slot
Operating Temperature	10 °C to 40 °C °C
Dimensions (W×H×D)	154 mm × 77 mm × 268 mm mm
Weight	2.3 kg

General Description & Compatibility

Compatible Mainframe	Keysight / Agilent 86100C Infiniium DCA-J
Required Mainframe Firmware	Revision A.08.10 or later
Number of Channels	2
Module Slot Occupancy	Double-wide (occupies two slots in the mainframe)
Measurement Modes Supported	Oscilloscope, Eye/Mask, Jitter, Amplitude

Vertical System

Electrical Bandwidth	> 32 GHz
RMS Noise Floor	< 300 µV (typical 250 µV at 32 GHz)
Nominal Input Impedance	50 Ω
Input Connector Type	2.4 mm (female)
Maximum Operating Input Voltage	±400 mV relative to channel offset
Maximum Safe Input Voltage	±2 V

Horizontal System & Timebase

Residual Jitter	< 100 fs RMS (60 fs RMS typical)

Clock Recovery & Triggering

Clock Recovery Operating Range	50 Mb/s to 14.2 Gb/s (continuous)
Clock Recovery Connection Mode	Single-connection triggerless operation
Loop Bandwidth Configuration	Adjustable loop bandwidth and peaking
Spread Spectrum Clocking (SSC) Tracking	Supported (exceeds industry standards)

Waveform Measurements & Analysis

PLL Characterization	Supported (includes Loop Bandwidth and Jitter Transfer)
Supported Jitter Measurements	Jitter decomposition (TJ, RJ, DJ)
Supported Amplitude Measurements	One/Zero levels, Peak-to-Peak, RMS noise, interference
Supported Time Measurements	Rise time, Fall time, Period, Frequency

Electrical Inputs

Input Coupling	DC

Dynamic Performance

Calculated Rise/Fall Time (10% to 90%)	< 11.0 ps (Option HBW) / < 26.9 ps (Option LBW)

Clock Recovery

Clock Recovery Frequency Range (Option 400)	Clock Recovery Frequency Range (Option 200) = 50 Mb/s to 14.2 Gb/s (continuous)
Clock Recovery Frequency Range (Option 100)	8.5 Gb/s to 14.2 Gb/s (continuous)
Supported Data Rates	50 Mb/s to 14.2 Gb/s (Option 200) / 8.5 Gb/s to 14.2 Gb/s (Option 100)
JTF Bandwidth Range	100 kHz to 8 MHz
Minimum Input Eye Opening for Lock	50 mV p-p
Consecutive Identical Digits Tolerance	1000 consecutive bits (at 10 Gb/s, typical)

Environmental

Storage Temperature Range	-40 °C to +70 °C
Maximum Operating Altitude	4600 m
Maximum Storage Altitude	15300 m
Operating Humidity Range	Up to 95% RH at 40 °C (non-condensing)

Compliance & Safety

Safety Compliance	IEC 61010-1, UL 61010-1, CAN/CSA-C22.2 No. 61010-1
EMC Compliance	IEC 61326-1, EN 61326-1

Performance

Calculated Rise/Fall Time (20% to 80%)	8.0 ps (standard 32 GHz, typical) / 5.1 ps (Option HBW 50 GHz, typical)

Timebase

Reference Clock Input Frequency Range	2.0 GHz to 13.5 GHz
Reference Clock Input Power Range	-10 dBm to +3 dBm

Triggering

Pattern Lock Support	Yes (requires 86100C/D mainframe with Option 001)

TECHNOLOGY

Sampling Oscilloscope and Waveform Analyzer

APPLICATIONS

High-speed digital communications, serial bus design validation (PCI-Express, SATA), and phase-locked loop (PLL) characterization