KEYSIGHT TECHNOLOGIES (AGILENT HP)

N4901B

The Keysight (Agilent) N4901B Serial BERT 13.5 Gb/s is an industry-leading bit error rate tester designed for high-performance serial bus characterization, transceiver testing, and semiconductor validation. Supporting data rates from 150 Mb/s to 13.5 Gb/s, the N4901B features integrated clock data recovery (CDR), advanced jitter injection capabilities, true differential inputs/outputs, and a comprehensive analysis measurement suite.

SPECIFICATIONS

General

Interfaces	GPIB, LAN, USB, VGA
Display	8.4-inch color LCD touch screen

Physical

Power Supply	100 to 240 V AC, 50 to 60 Hz
Operating Temperature	5 °C to 40 °C °C
Dimensions (W×H×D)	424 mm x 222 mm x 570 mm mm

System Architecture and Key Performance

Minimum Data Rate	150 Mb/s
Maximum Data Rate	13.5 Gb/s
Upgrade Capabilities	Upgradeable from 7 Gb/s to 13.5 Gb/s
Operating Modes	Pattern Generator, Error Detector
Chassis Configuration	Integrated Mainframe

Pattern Generator (TX) Specifications

Output Data Rate Range	150 Mb/s to 13.5 Gb/s
Output Transition Time (10% to 90%)	< 25 ps (20% to 80%)
Output Intrinsic Jitter	< 1 ps RMS (typical)
Output Amplitude Range	0.1 V to 1.8 Vp-p (single-ended), 0.2 V to 3.6 Vp-p (differential)

Error Detector (RX) Specifications

Input Data Rate Range	150 Mb/s to 13.5 Gb/s
Input Sensitivity (Differential)	< 50 mV pp
Input Interface Type	True differential inputs

Clocking and Clock Recovery

Integrated CDR Range 1	1.05 Gb/s to 1.6 Gb/s
Integrated CDR Range 2	2.11 Gb/s to 3.20 Gb/s
Integrated CDR Range 3	4.23 Gb/s to 6.40 Gb/s
Integrated CDR Range 4	9.9 Gb/s to 10.9 Gb/s

Jitter Injection and Tolerance

Jitter Modulation Range	200 ps
Jitter Modulation Frequency Range	DC to 1 GHz

Analysis and Software Features

Operating System	Windows XP
Measurement Suite Capabilities	Bathtub curve, output level, Q-factor, spectral jitter decomposition, fast eye mask, error location capture

Pattern Generator

PRBS Patterns	2^7-1, 2^10-1, 2^11-1, 2^15-1, 2^23-1, 2^31-1
User Pattern Memory	1 bit to 32,768,000 bits
PG Delay Control Range	-750 ps to +750 ps
Output Crossing Point Adjustment Range	20% to 80%

Clock and Delay

Clock Output Frequency Range	150 MHz to 13.5 GHz (option-dependent)
Clock Output Amplitude Range	0.1 Vp-p to 2.0 Vp-p (single-ended)
Sub-rate Clock Divider Ratios	2, 4, 8, 16

Error Detector

Error Detector Input Impedance	50 Ω (nominal)
Error Detector Input Voltage Range	-2.0 V to +3.0 V

Environmental

Storage Temperature Range	-40 °C to +70 °C

Generator Parameters

PG Output Offset Range	-2.00 V to +3.00 V
PG Output Termination Voltage Range	-2.00 V to +3.00 V
PG Output Transition Time (20% to 80%)	< 25 ps (20 ps typical)
PG Clock Output Offset Range	-2.00 V to +3.00 V
PG External Clock Input Frequency	150 MHz to 13.5 GHz
PG External Clock Input Amplitude	200 mVpp to 2.0 Vpp

Analyzer Parameters

ED Clock Input Frequency Range	150 MHz to 13.5 GHz
ED Data Input Threshold Range	-2.00 V to +3.00 V
ED Data Input Threshold Resolution	1 mV
ED Clock-to-Data Delay Resolution	100 fs
ED Auto-align Capabilities	Threshold and phase auto-alignment

Error Insertion

Error Insertion Rate Range	1.0 × 10^-2 to 1.0 × 10^-9

Sync & Trigger

Pattern Sync Output Amplitude	1 V nominal into 50 Ω
Trigger Output Amplitude	1 V nominal into 50 Ω

TECHNOLOGY

Bit Error Rate Testing (BERT)

APPLICATIONS

High-speed digital transceiver characterization, semiconductor design validation, telecom/datacom system testing