KEYSIGHT TECHNOLOGIES (AGILENT HP)

N4903A

The Keysight Technologies (formerly Agilent) N4903A J-BERT is a high-performance serial Bit Error Ratio Tester (BERT) designed for characterizing and testing receivers and transmitters in high-speed serial bus architectures up to 12.5 Gb/s.

SPECIFICATIONS

General

Interfaces	GPIB, LAN (10/100 Base-T), USB 2.0, VGA
Display	8.4-inch color LCD touch screen, 800 x 600 SVGA resolution
Target Standards Compliance	PCIe Gen1/Gen2, SATA, USB 3.0, DisplayPort, QPI, FB-DIMM, 10GbE

Physical

Power Supply	100 to 240 V AC (±10%), 50 to 60 Hz / 400 Hz, 450 VA maximum
Operating Temperature	5 °C to 40 °C °C
Dimensions (W×H×D)	424 mm × 222 mm × 563 mm mm
Weight	24.5 kg

Pattern Generator

Data Rate Range (Option C07)	150 Mb/s to 7.0 Gb/s
Data Rate Range (Option C12.5)	150 Mb/s to 12.5 Gb/s (Option C13)
Output Connector Type	2.4 mm (f)
Output Amplitude Range	0.10 V to 1.8 V (single-ended) or 0.20 V to 3.6 V (differential)
Amplitude Resolution	5 mV
Transition Time (20% - 80%)	< 25 ps
Output Impedance	50 Ohm
Termination Voltage Range	-2.0 V to +3.0 V
Offset Voltage Range	-2.0 V to +3.0 V
PRBS Pattern Lengths	2^7-1, 2^10-1, 2^11-1, 2^15-1, 2^23-1, 2^31-1
User Pattern Memory Depth	32 Mbit per channel

Error Detector

Input Rate Range (Option C07)	150 Mb/s to 7.0 Gb/s
Input Rate Range (Option C12.5)	150 Mb/s to 12.5 Gb/s (Option C13)
Input Connector Type	2.4 mm (f)
Input Impedance	50 Ohm
Input Sensitivity	50 mV (typical)
Maximum Input Amplitude	2.0 V
Threshold Range	-2.0 V to +3.0 V
Threshold Resolution	1 mV
Clock Input Frequency Range	150 MHz to 12.5 GHz (Option C13 dependent)
Clock Input Amplitude Range	100 mV to 1.2 V

Jitter Generation

Sinusoidal Jitter (SJ) Frequency Range	10 Hz to 80 MHz
Random Jitter (RJ) Frequency Range	10 kHz to 1 GHz
Bounded Uncorrelated Jitter (BUJ) Rate Range	10 Mb/s to 3.2 Gb/s
Jitter Suite Option	Option J12 (Jitter Source with RJ, LF-RJ, PJ, SJ, BU)

Clock Output

Clock Output Frequency Range (Option C07)	150 MHz to 7.0 GHz
Clock Output Frequency Range (Option C12.5)	150 MHz to 12.5 GHz (Option C13)
Clock Output Amplitude Range	0.10 V to 1.8 V
Clock Output Interface	2.4 mm (f)

System Architecture

Internal Operating System	Windows XP Professional

Interfaces & Connectivity

Trigger Output Connector	SMA (f)
Trigger Input Connector	SMA (f)
External Reference Input	10 MHz (BNC)
External Reference Output	10 MHz (BNC)

Physical & Environmental

Storage Temperature Range	-40 °C to +70 °C
Warm-up Time	30 minutes

Standards & Compliance

Recommended Calibration Cycle	1 Year

Delay Control

Data-to-Clock Delay Range	±750 ps
Data-to-Clock Delay Resolution	100 fs

Pattern Generator Specs

Sub-rate Clock Output Ratio	1/2, 1/4, 1/8, 1/16 of data rate
Pattern Sync Output Connector	SMA (f), 50 Ohm
Pattern Generator Intrinsic Random Jitter	< 250 fs RMS (typical)

Jitter Injection

SSC Modulation Frequency Range (Option J11)	30 kHz to 33 kHz
SSC Modulation Amplitude Range (Option J11)	0% to 0.5% (down-spread), -0.25% to +0.25% (center-spread)
Random Jitter (RJ) Amplitude Range (Option J10)	0 to 15.7 ps RMS (data rate dependent)
Bounded Uncorrelated Jitter (BUJ) Amplitude Range (Option J10)	0 to 220 ps peak-to-peak
Sinusoidal Jitter (SJ) Amplitude Range (Option J10)	0 to 220 ps peak-to-peak (high frequency), up to 16 ns (low frequency)

Error Detector Specs

Error Detector Auxiliary Output	Selectable: Error pulse, block trigger, or clock/16

Environmental

Operating Humidity Range	5% to 90% relative humidity (non-condensing)

Power

Power Consumption (Maximum)	550 VA

TECHNOLOGY

High-Performance Serial Bit Error Ratio Testing (BERT)

APPLICATIONS

Receiver characterization, transmitter testing, jitter tolerance testing, and signal integrity analysis for high-speed serial buses.