KEYSIGHT TECHNOLOGIES (AGILENT HP)

U4154A

The Keysight Technologies U4154A is an AXIe-based logic analyzer module designed for reliable measurements on high-speed digital systems and DDR memory buses operating up to 4 Gb/s. Capable of performing state analysis with data valid windows as small as 100 ps by 100 mV, and asynchronous timing analysis up to 5 GHz, it provides comprehensive insight with a 12.5 GHz TimingZoom mode and up to 200 M samples of memory per channel.

SPECIFICATIONS

General

Interfaces	AXIe backplane interface, Multiframe expansion port
Display	None (headless module; requires mainframe or external PC host display)

Physical

Power Supply	Powered via AXIe backplane (48 VDC nominal), 155 W maximum power consumption
Operating Temperature	0 to 50 °C °C
Dimensions (W×H×D)	30 mm × 322.3 mm × 281.5 mm mm
Weight	3.12 kg kg

Acquisition Specifications

Maximum State Data Rate (136 channels)	2.5 Gb/s
Maximum State Data Rate (68 channels)	4 Gb/s
Typical Maximum State Clock Frequency	2.5 GHz
Typical Minimum State Clock Frequency (Single Edge)	12.5 MHz
Typical Minimum State Clock Frequency (Both Edges)	6.25 MHz
Typical Sample Position Adjustment Resolution	5 ps
Typical Minimum Data Valid Window	100 ps
Typical Minimum Setup Time	50 ps
Typical Minimum Hold Time	50 ps
Typical Minimum Eye Height	100 mV
Typical Sample Position Adjustment Range	7 ns
Typical Minimum State Clock Pulse Width	200 ps
Nominal Number of Clocks	2
Typical Minimum Time Between Active Clock Edges	400 ps
Typical Maximum Time Between Active Clock Edges	80 ns
Nominal Number of Clock Qualifiers	4
Typical Clock Qualifier Setup Time	100 ps
Typical Clock Qualifier Hold Time	100 ps
Typical Time Tag Resolution	80 ps
Typical Maximum Time Count Between Stored States	66 days
Nominal Maximum Timing Sample Rate (Half-Channel)	5 GHz
Nominal Maximum Timing Sample Rate (Full-Channel)	2.5 GHz
Nominal Minimum Timing Sample Period (Half-Channel)	200 ps
Nominal Minimum Timing Sample Period (Full-Channel)	400 ps
Conventional Timing Deep Analysis Memory Depth	200 M samples (half-channel) / 100 M samples (full-channel)
Transitional Timing Sample Rate	2.5 GHz
TimingZoom Sampling Rate	12.5 GHz (80 ps)
TimingZoom Memory Depth	256 Ksamples
Number of State/Timing Channels (Single Module)	68 (half-channel) / 136 (full-channel)

Number of State/Timing Channels (Two Modules Combined)	136 (half-channel) / 272 (full-channel)
Nominal Pod Usage in Half-Channel Mode	1 pod from each odd/even pair (user selectable)
Nominal Pod Usage in Full-Channel Mode	All pods in use
Nominal Maximum Time Between Transitions	66 days
Typical Minimum Data Pulse Width	1 sample period + 200 ps
Optional Memory Depth Capacities	2M, 4M, 8M, 16M, 32M, 64M, 128M, 200M (configuration dependent)

Triggering Specifications

Typical Maximum Trigger Sequence Speed	2500 MHz (400 ps)
Nominal Trigger Pattern Recognizers	16 patterns (evaluated as =, !=, >, >=, <, <=)
Nominal Trigger Range Recognizers	4 double-bounded ranges (evaluated as in range, not in range)
Nominal Trigger Edge Detectors (Timing Mode)	16
Nominal Trigger Edge Detectors (Transitional Timing Mode)	16
Nominal Trigger Occurrence Counter	1 per sequence level (up to 999,999,999)
Nominal Trigger Timers	2
Nominal Trigger Flags	4
Nominal Trigger Arm Inputs	1
Nominal Trigger Boolean Conditions	Arbitrary Boolean combinations
Timer Actions	Start from reset, Stop and reset, Pause, Resume
Flag Actions	Set, Clear, Pulse set, Pulse clear
Nominal Maximum Trigger Sequence Levels	16
Nominal Trigger Sequence Level Branching	Arbitrary 8-way branching
Nominal Trigger Position	Start, center, end, or user-defined
Nominal Maximum Pattern Width (Single Label)	136 bits
Nominal Maximum Pattern Width (Two-Card Set)	272 bits (AND of multiple labels)
Nominal Maximum Range Width	64 bits
Nominal Timer Range (Timing Modes)	100 ns to 27 hours
Nominal Timer Range (State Mode)	200 * state clock period to 27 hours
Nominal Timer Reset Latency (Timing Modes)	40 ns
Nominal Timer Reset Latency (State Mode)	80 * state clock period

Signal Integrity & Probing

Supported Probe Types	Compatible with 90-pin logic analyzer probes
Signal Support & Thresholds	Single-ended and differential support, adjustable thresholds
Eye Diagram Capability	Simultaneous eye diagrams on all channels with automated sample position setup

System Integration & Mainframe Compatibility

Mainframe Compatibility	Compatible with AXIe chassis (e.g., M9502A, M9505A)
Multi-Module Synchronization	Combine up to 2 modules for 272 channels on a single time base and trigger

Ordering Options - State Speed

Option 01G State Speed	1.4 Gb/s
Option 02G State Speed	2.5 Gb/s
Option 04G State Speed	4.0 Gb/s

Ordering Options - Memory Depth

Option 002 Memory Depth	2 M samples
Option 004 Memory Depth	4 M samples
Option 008 Memory Depth	8 M samples
Option 016 Memory Depth	16 M samples
Option 032 Memory Depth	32 M samples
Option 064 Memory Depth	64 M samples
Option 128 Memory Depth	128 M samples

Environmental

Non-Operating Temperature Range	-40 to +70 °C
Operating Altitude	Up to 3,000 meters

Physical Specification

Module Format	AXIe 1.0 (1-slot instrument module)

State/Timing Performance

Voltage Threshold Range	-3.0 V to +5.0 V
Threshold Setting Resolution	5 mV
Threshold Accuracy	±(30 mV + 1% of setting)

System Integration

AXIe Compliance	AXIe-1.0 Base Architecture
Required Slot Width	1 slot
Supported Mainframes	Keysight M9502A (2-slot), M9505A (5-slot)
Maximum Multi-Module Configuration	Up to 3 modules (408 channels in full-channel mode)
Module Warm-up Time	30 minutes

Power and Environmental

Maximum Power Dissipation	195 W
Shock (Non-Operating)	30 g, trapezoidal, 11 ms
Vibration (Operating)	0.21 g (rms), 5 Hz to 500 Hz (random)
Vibration (Non-Operating)	2.09 g (rms), 5 Hz to 500 Hz (random)

Software & Interface

Host Software Requirements	Keysight Logic and Protocol Analyzer software v5.40 or higher
Operating System Compatibility	Windows 7 (64-bit), Windows 10 (64-bit)

Physical & Interfaces

Input Connectivity	Four 160-pin connectors on front panel

TECHNOLOGY

Logic Analyzer

APPLICATIONS

DDR Memory Validation and High-Speed Digital System Debugging