KEYSIGHT TECHNOLOGIES (AGILENT HP)

M8020A

The Keysight M8020A J-BERT is a highly integrated, modular high-performance bit error ratio tester (BERT) designed for fast and accurate receiver characterization of high-speed digital devices operating up to 8.5, 16, or 32 Gb/s.

SPECIFICATIONS

General

Interfaces	LAN (LXI-C compliant), USB, PCIe (via AXIe backplane / external controller)
Display	None (headless modular system, controlled via external PC / monitor using M8000 System Software)
Chassis Compatibility	AXIe
Supported Standards	PCIe, USB, MIPI, SATA, DisplayPort, SAS, HDMI

Physical

Power Supply	100 to 240 VAC, 50 to 60 Hz (supplied by host AXIe mainframe such as M9502A or M9505A)
Operating Temperature	5 to 40 °C °C

Core Signal and Electrical Performance

Maximum Data Rate (Option C08)	Up to 8.5 Gb/s
Maximum Data Rate (Option C16)	Up to 16.2 Gb/s
Maximum Data Rate (Option G32)	Up to 32.4 Gb/s (Option C32)
Frequency Resolution	1 Hz
Generator Channels	Up to 4 channels
Generator Differential Output Amplitude	100 mVpp to 2.4 Vpp
Error Detector Input Sensitivity	< 50 mVpp (typical at 16 Gb/s)

Measurement Capabilities and Timing

Receiver Equalization	Integrated CTLE (Continuous Time Linear Equalizer), interactive DFE (Decision Feedback Equalizer)

RF and Passive Transmission Characteristics

Integrated Jitter Sources	Random Jitter (RJ), Periodic Jitter (PJ), Sinusoidal Jitter (SJ), Bounded Uncorrelated Jitter (BUJ), Spread Spectrum Clocking (SSC)
Spread Spectrum Clocking (SSC) Range	Triangle or sine modulation, 30 to 33 kHz, up to 5000 ppm

Physical and Mechanical Attributes

Form Factor	AXIe modular system (utilizes M8041A High-Performance BERT Controller Module and M8051A Extension Module)

User Interface and Software Control

Software Control	Keysight M8000 System Software (running on external PC or embedded AXIe controller)

Pattern Generator

Generator Single-Ended Output Amplitude	50 mVpp to 1.2 Vpp
Generator Output Amplitude Resolution	1 mV
Generator Transition Time (20% to 80%)	< 16 ps
Supported PRBS Patterns	2^7-1, 2^9-1, 2^10-1, 2^11-1, 2^15-1, 2^23-1, 2^31-1, 2^58-1, 2^63-1
User Pattern Depth	Up to 2 Gb (configuration dependent)

Error Detector

Integrated CDR Frequency Range	1.1 Gb/s to 16.2 Gb/s (option dependent)
ED CTLE Peaking Range	0 dB to 12 dB
ED DFE Support	1-tap
ED CDR Loop Bandwidth	up to 20 MHz
Error Detector Auto-Alignment	Automatic adjustment of phase and threshold

Jitter Emulation

Delay Control Range	220 ps
Delay Control Resolution	50 fs
Random Jitter (RJ) Range	0 to 15.7 ps RMS
Periodic Jitter (PJ) Range	0 to 220 ps
PJ Frequency Range	100 Hz to 100 MHz
SSC Frequency Range	30 kHz to 33 kHz

Physical & Environmental

AXIe Slot Requirement	3 slots for M8041A module, 2 slots for M8051A module

TECHNOLOGY

Bit Error Ratio Testing (BERT)

APPLICATIONS

Receiver characterization and compliance testing for high-speed digital buses such as PCIe, USB, MIPI, SATA/SAS, and DisplayPort