KEYSIGHT TECHNOLOGIES (AGILENT HP)

N4960A

The Keysight N4960A Serial BERT is a high-performance, compact bit error rate tester designed for characterization and compliance testing of high-speed digital systems up to 32 Gb/s. By separating the controller mainframe from the remote pattern generator and error detector heads, the system minimizes cable losses and maximizes signal integrity at the device under test.

SPECIFICATIONS

General

Interfaces	USB 2.0, LAN
Display	None (controlled via external PC with N4960A software)
AC Input Voltage	100 to 240 VAC
AC Input Frequency	50 to 60 Hz
Power Consumption (Maximum)	150 VA
Warm-up Time	30 minutes

Physical

Power Supply	100 to 240 V AC, 50/60 Hz
Operating Temperature	10 to 40 °C °C
Dimensions (W×H×D)	220 mm × 89 mm × 345 mm mm
Weight	4.8 kg kg
Chassis Height	2U

System Architecture and Key Performance

Data Rate Range (Option 17)	1.5 Gb/s to 17.0 Gb/s
Data Rate Range (Option 32)	1.5 Gb/s to 32.0 Gb/s
Chassis Configuration	Controller mainframe with remote heads
Supported Remote Heads	N4951A/B Pattern Generator, N4952A Error Detector

Pattern Generator (TX) Specifications

Pattern Generator PRBS Types	PRBS 7, PRBS 9, PRBS 10, PRBS 11, PRBS 15, PRBS 23, PRBS 31
User-Defined Pattern Memory Depth	Up to 8 Mb (8,388,608 bits)

Jitter Injection and Tolerance

Jitter Injection Source	Integrated clock source with jitter (with Option CJ0)
Sinusoidal Jitter (SJ) Frequency Range	10 kHz to 100 MHz
Random Jitter (RJ) Source	Supported (with Option CJ0)
Bounded Uncorrelated Jitter (BUJ) Source	Supported (with Option CJ0)
Spread Spectrum Clocking (SSC) Support	Supported (with Option CJ0)

Error Detector (RX) Specifications

Auto-Alignment Range	Automated clock-to-data alignment
Input Data Impedance	50 Ω nominal

Clocking and Clock Recovery

External Reference Clock Input	10 MHz
Internal Reference Clock Output	10 MHz

Physical and Environmental

Form Factor	Benchtop (2U, half-rack width)
Cooling Mechanism	Active fan cooling
Storage Temperature Range	-40 °C to +70 °C
Operating Humidity Range	15% to 95% relative humidity (non-condensing)

Power and Compliance

Recommended Calibration Interval	1 year

Reference Clock

Internal Reference Clock Accuracy	±1.5 ppm
External Reference Input Frequency	10 MHz
External Reference Input Level	100 mV to 2.0 V p-p
External Reference Input Impedance	50 Ω (nominal)
Reference Output Frequency	10 MHz
Reference Output Level	1.0 V p-p (into 50 Ω)

Clock Generation

Internal Clock Resolution	1 kHz
Internal Clock Frequency Range (Option 17)	9.5 to 17.0 GHz
Internal Clock Frequency Range (Option 32)	9.5 to 32.0 GHz

Jitter Injection

Random Jitter (RJ) Range	0 to 15.6 mUI (RMS)
Sinusoidal Jitter (SJ) Maximum Amplitude	110 UI (at 100 Hz)
Bounded Uncorrelated Jitter (BUJ) Range	0 to 0.5 UI (peak-to-peak)
Spread Spectrum Clocking (SSC) Modulation Frequency	30 to 33 kHz
Spread Spectrum Clocking (SSC) Deviation Range	0 to -0.5% (downspread)

Error Analyzer

Error Analyzer PRBS Types	PRBS 2^7-1, 2^9-1, 2^11-1, 2^15-1, 2^23-1, 2^31-1

Measurements

Measurement Capabilities	Bit Error Ratio (BER), Error Count, Error Interval, Error-Free Interval

Interfaces

Remote Head Interface	Dedicated high-density control cables

TECHNOLOGY

Serial BERT

APPLICATIONS

High-Speed Digital Receiver and Transmitter Characterization