STANFORD RESEARCH SYSTEMS

SR830

The Stanford Research Systems SR830 is a dual-phase DSP Lock-In Amplifier designed for high-performance scientific and engineering measurements. Operating over a frequency range of 1 mHz to 102.4 kHz, it offers more than 100 dB of dynamic reserve without pre-filtering, exceptional stability of 5 ppm/°C, and 0.01 degree phase resolution. Leveraging advanced digital signal processing (DSP) architecture, the SR830 replaces the conventional analog demodulators and filters of legacy instruments to provide outstanding noise rejection and measurement accuracy.

SPECIFICATIONS

General

Interfaces	GPIB (IEEE-488.2), RS-232
Display	Dual 4.5-digit LED displays with 40-segment LED bar graphs
Preamplifier Power Output Voltage	±15 VDC
Preamplifier Power Output Current	100 mA (maximum)

Physical

Power Supply	100/120/220/240 VAC, 50/60 Hz, 40 W
Operating Temperature	0 to 50 °C °C
Dimensions (W×H×D)	432 × 133 × 495 mm (17" × 5.25" × 19.5") mm
Weight	13.6 kg (30 lbs) kg

Signal Channel

Input Configuration	Single-ended (A) or differential (A-B)
Input Impedance (Voltage)	10 MΩ + 25 pF, AC or DC coupled
Input Impedance (Current)	1 kΩ or 100 Ω to virtual ground (gain dependent)
Full-Scale Sensitivity Range	2 nV to 1 V (voltage), 2 fA to 1 µA (current)
Frequency Range	1 mHz to 102.4 kHz
Voltage Input Noise	6 nV/√Hz at 1 kHz
Current Input Noise	13 fA/√Hz at 1 kHz (10^8 V/A gain), 130 fA/√Hz at 1 kHz (10^6 V/A gain)
Common Mode Rejection Ratio (CMRR)	100 dB to 10 kHz (differential input, decreases by 20 dB/decade above 10 kHz)
Dynamic Reserve	>100 dB (without pre-filtering)
Maximum Input Voltage	50 V peak (damage threshold)
Gain Accuracy	±1% (typical)
Gain Stability	<200 ppm/°C
Input Coupling	AC or DC (AC cutoff at 0.16 Hz)
Input Shield Grounding Options	Float (10 kΩ to ground) or Ground
Line Notch Filters	50/60 Hz and 100/120 Hz

Reference Channel

Reference Frequency Range	1 mHz to 102.4 kHz
Reference Input Impedance	1 MΩ, AC coupled
Reference Input Voltage Range	Sine (>100 mVpk) or TTL (>2 V)
Phase Resolution	0.01°
Phase Accuracy	<1° (absolute phase error)
Phase Noise	<0.0001° rms at 1 kHz
Phase Drift	<0.01°/°C below 10 kHz, <0.1°/°C above 10 kHz
Acquisition Time (Lock Time)	(2 cycles + 5 ms) or 40 ms, whichever is larger
Harmonic Detection Capabilities	nF up to 102.4 kHz (n < 19,999)

Internal Oscillator

Oscillator Frequency Range	1 mHz to 102.4 kHz
Oscillator Frequency Resolution	4.5 digits or 0.1 mHz, whichever is larger
Oscillator Frequency Accuracy	25 ppm + 30 µHz
Oscillator Output Amplitude Range	4 mVrms to 5 Vrms
Oscillator Output Amplitude Resolution	2 mVrms
Oscillator Output Amplitude Accuracy	±1%
Oscillator Output Amplitude Stability	0.05%/°C
Oscillator Output Distortion (THD)	-80 dBc at f < 10 kHz, -70 dBc at f > 10 kHz (1 Vrms amplitude)
Oscillator Output Impedance	50 Ω
Oscillator Output Waveforms Available	Sine

Demodulator and Filtering

DSP Architecture / Processing Resolution	16-bit A/D conversion at 256 kHz, 24-bit DSP
Time Constant Range	10 µs to 30 ks
Low-Pass Filter Roll-off Slopes	6, 12, 18, 24 dB/octave
Synchronous Filtering Option	Available below 200 Hz
DC Drift of Outputs	<5 ppm/°C (for stable dynamic reserve)

Auxiliary Inputs and Outputs

Auxiliary A/D Input Channels	4 channels
Auxiliary A/D Input Voltage Range	±10.24 V
Auxiliary A/D Resolution and Sampling Rate	16-bit (1/3 mV resolution) at 512 Hz
Auxiliary D/A Output Channels	4 channels
Auxiliary D/A Output Voltage Range	±10.24 V
Auxiliary D/A Resolution	16-bit (1/3 mV resolution)
Data Buffer Size	16,384 points per channel (two buffers)
Maximum Data Sampling Rate	512 Hz (internally triggered)
Analog Outputs (X, Y, R, Theta)	Front-panel CH1 and CH2 outputs (±10 V, 50 Ω impedance)

Interfaces and External Control

GPIB Interface Support	IEEE-488.2 standard
RS-232 Interface Support	Standard, up to 19.2 kbaud
Preamplifier Power Port Specification	±15 V, 100 mA (rear panel, for SRS preamps)
Trigger Inputs	TTL level (starts data buffer)
TTL Reference Output	0 to 5 V TTL square wave (front panel)

Display and Front Panel

Display Type	Dual 4.5-digit LED displays with two 40-segment LED bar graphs
Channel 1 Display Parameters	X, R, X Noise, Aux 1, Aux 2
Channel 2 Display Parameters	Y, Theta, Y Noise, Aux 3, Aux 4

Physical and Environmental

Rack Mounting Option Details	19" rack mountable (3U height, rack ears optional)

Power Specifications

AC Line Voltage Requirements	100, 120, 220, 240 VAC (switch selectable)
AC Line Frequency Range	50/60 Hz
Power Consumption	40 W

Reference Section

Phase Orthogonality	90° ± 0.001°

Auxiliary Inputs & Outputs

Auxiliary A/D Input Impedance	1 MΩ
Auxiliary D/A Output Impedance	<1 Ω
Auxiliary D/A Output Current	10 mA (maximum)
Auxiliary D/A Output Accuracy	±(0.1% of setting + 10 mV)
Auxiliary A/D Input Accuracy	±(0.1% of reading + 10 mV)

Inputs & Outputs

Trigger Input Impedance	10 kΩ
Trigger Input Minimum Pulse Width	1 µs

Signal Input

Line Notch Filter Q-Factor	10
Line Notch Filter Attenuation	50 dB

Outputs

CH1 and CH2 Analog Output Range	±10 V (full scale)
CH1 and CH2 Analog Output Impedance	<1 Ω
CH1 and CH2 Output Update Rate	512 Hz

Interfaces

GPIB Command Compatibility	IEEE-488.2
RS-232 Baud Rates	300, 1200, 2400, 4800, 9600, 19200 bps

Signal Processing

X, Y Offset Range	±105% of full scale
X, Y Expand Options	×1, ×10, or ×100

Accessories

Supported Preamplifiers	SR550 (voltage), SR552 (voltage), SR554 (transformer)

TECHNOLOGY

DSP (Digital Signal Processing) Dual-Phase Lock-In Amplifier

APPLICATIONS

Precision phase-sensitive voltage and current measurement, low-level signal recovery