

TEKTRONIX

AWG710B

The Tektronix AWG710B is a high-performance Arbitrary Waveform Generator designed for simulating real-world signals at extreme speeds. Combining a sample rate of up to 4.2 GS/s, an outstanding 2.0 GHz analog bandwidth, and an extensive 32.4 M point record length, the AWG710B is engineered to meet the demanding requirements of high-speed digital, communications, and semiconductor device testing.

SPECIFICATIONS

General

Interfaces	GPIB (IEEE 488.2), LAN (10Base-T/100Base-TX), RS-232, VGA, Keyboard (PS/2), Mouse (PS/2), PC Card (Type II PCMCIA)
Display	10.4-inch TFT color LCD, 640 × 480 pixels

Physical

Power Supply	100 to 240 V AC, 47 to 63 Hz, 380 VA maximum
Operating Temperature	10 to 40 °C °C
Dimensions (W×H×D)	425 mm × 245 mm × 493 mm mm
Weight	19.0 kg

Channels & Sample Rate

Number of Analog Channels	1
Maximum Sample Rate	4.2 GS/s
Minimum Sample Rate	10.0 MS/s
Vertical Resolution	8 bits
Maximum Arbitrary Memory Depth	32.4 M points (32,400,000 points)
Sample Rate Accuracy	±1 ppm

Signal Fidelity & Frequency Response

Analog Bandwidth	2.0 GHz (-3 dB, direct output)
Rise/Fall Time (Direct Output)	< 175 ps (20% to 80%)
Rise/Fall Time (Normal Output)	< 280 ps (20% to 80%)

Analog Output Parameters

Output Impedance	50 Ω
Output Coupling	DC
Amplitude Range (Normal Output)	50 mVp-p to 2.0 Vp-p (differential into 50 Ω)
Amplitude Range (Direct Output)	20 mVp-p to 1.0 Vp-p (differential into 50 Ω)
Amplitude Resolution	1 mV
DC Offset Range	± 0.5 V (into 50 Ω , normal output)
Output Connector Type	SMA (front panel)

Marker & Auxiliary Outputs

Number of Marker Channels	2
Marker Amplitude Range	0.5 Vp-p to 2.0 Vp-p into 50 Ω
Marker Delay Adjustment Range	0 to 2.0 ns
Marker Delay Resolution	1 ps
Marker Output Connector Type	SMA (front panel)

Run Modes & Sequencing

Operating Modes	Continuous, Triggered, Gated, Sequence
Maximum Sequence Steps	8,000 steps
Loop Count Range	1 to 65,536 or Infinite
Waveform Segment Length Granularity	1 point
Minimum Waveform Segment Length	1 point

Clock & Triggering

Internal Clock Reference Frequency	10 MHz
External Reference Clock Input Frequency	10 MHz
Trigger Input Impedance	50 Ω or 1 k Ω
Trigger Input Threshold Range	-5.0 V to +5.0 V
Trigger Input Minimum Pulse Width	5 ns
Trigger Input Connector Type	BNC (front panel)

System, Control & Connectivity

Internal Operating System	VxWorks
Hard Disk Drive	20 GB (or larger)
Floppy Disk Drive	3.5-inch, 1.44 MB
External Monitor Port	15-pin D-sub (VGA)
PC Card Slot	Type II PCMCIA (front panel)

Physical Characteristics

Chassis Form Factor	Benchtop
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Power Specifications

AC Input Voltage Range	100 to 240 V AC
AC Input Frequency Range	47 to 63 Hz

Environmental & Compliance

Storage Temperature Range	-20 to +60 °C
Operating Humidity Range	20% to 80% RH (non-condensing)
Operating Altitude	Up to 3,000 m

Spectral Purity

SFDR (Direct Output)	-55 dBc @ 10 MHz, -45 dBc @ 100 MHz, -35 dBc @ 500 MHz
Phase Noise	-90 dBc/Hz @ 10 kHz offset (typical, 10 MHz output)

Clock & Reference

External Clock Input Amplitude	0.4 Vp-p to 2.0 Vp-p
External Reference Input Amplitude	0.2 Vp-p to 3.0 Vp-p
External Reference Input Impedance	50 Ω (AC coupled)

Auxiliary Inputs

Auxiliary Add Input Bandwidth	DC to 100 MHz
Auxiliary Add Input Impedance	50 Ω
Auxiliary Add Input Range	± 1.0 V

Trigger & Event

Event Input Impedance	1 k Ω (pulled up to +5 V)
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Marker Outputs

Marker Rise/Fall Time	< 130 ps (20% to 80%)
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Power

Power Consumption	360 VA maximum
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Environmental

Operating Vibration	0.27 G RMS (5 Hz to 500 Hz)
Non-Operating Vibration	2.28 G RMS (5 Hz to 500 Hz)
Non-Operating Shock	294 m/s ² (30 G), half-sine, 11 ms duration

Options

Memory Option (Option 01)	64 MS (64,800,000 points)
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Analog Output

Low Pass Filters	20 MHz, 50 MHz, 100 MHz, 200 MHz (selectable for Normal Output)
Amplitude Accuracy (Normal Output)	±(1.5% of setting + 10 mV) at 0 V Offset
Amplitude Accuracy (Direct Output)	±(1.5% of setting + 2 mV)
DC Offset Accuracy	±(2.0% of offset + 10 mV) at minimum amplitude (Normal Output)
Harmonic Distortion (Normal Output)	≤ -50 dBc (at 10 MHz, 1.0 Vp-p, typical)
Spurious Noise (Normal Output)	≤ -55 dBc (at 10 MHz, 1.0 Vp-p, 10 MHz to 4.2 GHz, typical)

Clock & Trigger

Trigger to Output Delay	70 ns (Direct Output) / 100 ns (Normal Output) plus 1 clock cycle (typical)
Event Input Minimum Pulse Width	1280 master clock cycles
Event Input Connector Type	BNC (rear panel)
Reference Clock Output Amplitude	1.2 Vp-p into 50 Ω
Reference Clock Output Connector Type	BNC (rear panel)

Markers

Marker Output Impedance	50 Ω
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Interfaces

Keyboard Port	PS/2 (6-pin mini-DIN)
Mouse Port	PS/2 (6-pin mini-DIN)

Compliance & Environmental

Safety Standards	UL 3111-1, CSA C22.2 No. 1010.1, EN 61010-1, IEC 61010-1
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