TEKTRONIX

TLA5203 Opt. 7S

The Tektronix TLA5203 Opt. 7S is a high-performance 102-channel logic analyzer from the TLA5000 Series, equipped with Option 7S to deliver an expanded deep memory capability of 32 Mb at 2 GHz (500 ps) timing resolution. Designed for advanced digital system debugging and analysis, it features simultaneous 125 ps MagniVu timing resolution on all channels and a integrated 10.4-inch XGA display. Built on a Windows XP platform, it supports high-speed state acquisition up to 235 MHz alongside time-correlated analog-digital viewing (iView) with compatible Tektronix oscilloscopes.

SPECIFICATIONS

General

Interfaces	1x 10/100 Base-T Ethernet (RJ-45), 4x USB 2.0 (2 front, 2 rear), 1x GPIB (IEEE-488), 1x RS-232-C (9-pin), 1x Parallel (Centronics 25-pin), 2x PS/2 (keyboard/mouse), 1x SVGA output (15-pin D-sub)
Display	10.4 in. Active-Matrix Color TFT LCD, 1024 x 768 (XGA) resolution

Physical

Power Supply	90 V to 250 V AC, 45 Hz to 66 Hz, 300 W maximum
Operating Temperature	+5 °C to +45 °C °C
Dimensions (W×H×D)	437 mm × 285 mm × 401 mm mm
Cooling Clearance	51 mm (2 in.) on sides and rear

Acquisition Specifications

Number of Channels	102 (96 data, 6 clock/qualifier)
Maximum State Clock Rate	235 MHz
Maximum Timing Sample Rate (Half Channel)	2.0 GHz (500 ps)
Maximum Timing Sample Rate (Full Channel)	1.0 GHz (1.0 ns)
MagniVu Timing Resolution	125 ps (8 GHz)
Record Length / Memory Depth (Per Channel)	32 Mb (Option 7S)
MagniVu Record Length	16 Kb per channel
Setup and Hold Window	1.5 ns (across all channels)

Triggering System

Trigger State Sequences	16 states
Trigger Word Recognizers	16 word recognizers
Trigger Range Recognizers	4 range recognizers
Counter/Timers	Two 48-bit counter/timers, 8 ns resolution
Glitch/Violation Triggering	Glitch and Setup/Hold violation triggering and display
Trigger Position	Anywhere in record (0% to 100% pre-trigger/post-trigger)

Probing & Input Characteristics

Supported Probe Interfaces	Tektronix P64xx series (e.g., P6417, P6418, P6419, P6434)
Input Impedance (P6417/18/19)	20 kOhm / 2.0 pF
Threshold Range	-2.0 V to +4.5 V
Threshold Accuracy	+/- (35 mV + 1% of threshold setting)
Threshold Resolution	10 mV
Maximum Input Voltage	+/- 15 V
Minimum Input Voltage Swing	300 mV

System & Processing

Operating System	Windows XP Professional
Processor Type	Intel Celeron 2.0 GHz
System Memory (RAM)	512 MB DDR (expandable to 1 GB)
Storage Capacity (HDD)	80 GB (or larger)
Removable Media	Internal CD-RW/DVD-ROM drive

Display & User Interface

Display Size	10.4 in. (26.4 cm)
Display Resolution	1024 x 768 pixels
Display Type	Active-Matrix Color TFT LCD
External Display Output	SVGA (15-pin D-sub, supports up to 1600x1200 resolution)

External Connections & Ports

LAN Interface	10/100 Base-T RJ-45
USB Ports	4x USB 2.0 (2 front, 2 rear)
GPIB Interface	IEEE-488
RS-232 Interface	9-pin D-sub male
Parallel Interface	Centronics 25-pin D-sub female
PS/2 Ports	2x PS/2 (1 keyboard, 1 mouse)
External Trigger Input	BNC, female
External Trigger Output	BNC, female

Software & Analysis Capabilities

Time-Correlated Views	iView (Time-correlated digital-analog view with external oscilloscope)
Supported iView Oscilloscopes	Tektronix TDS3000, TDS5000, TDS6000, TDS7000, CSA7000 series
Export Data Formats	ASCII, CSV, binary
Remote Control Interface	TLA Programmatic Interface (via TCP/IP or GPIB)

Power & Physical Characteristics

Power Requirements	90 V to 250 V AC, 45 Hz to 66 Hz
Power Consumption	300 W maximum
Form Factor	Benchtop (rackmountable via optional TLA5000 Rackmount Kit)
Height	285 mm
Width	437 mm
Depth	401 mm
Weight (Without Probes)	12.0 kg (26.5 lb.)

Environmental & Compliance

Storage Temperature	-20 °C to +60 °C
Operating Humidity	20% to 80% non-condensing
Operating Altitude	Up to 3,000 m (10,000 ft.)
Non-Operating Altitude	Up to 12,190 m (40,000 ft.)
Safety Certifications	UL61010B-1, CAN/CSA C22.2 No. 1010.1, EN61010-1
EMC Compliance	EN61326, FCC Part 15 Class A
Operating Vibration	0.31 g RMS (5 Hz to 500 Hz)
Non-Operating Vibration	2.46 g RMS (5 Hz to 500 Hz)
Operating Shock	290 m/s^2 (30 g), half-sine, 11 ms duration
Acoustic Noise	51 dBA (typical)

Acquisition System

Number of Clock Channels	4 single-ended
Number of Qualifier Channels	2
Minimum State Clock Pulse Width	2.0 ns
Timing Acquisition Sample Period Range	2 ns to 50 ms

Trigger System

Maximum Trigger Sequencer Rate	235 MHz
Trigger Actions	Trigger, Go To, Set/Clear Signal, Start/Stop/Reset Timer, Increment/Decrement Counter, Store/Don't Store

Analog Multiplexer

Analog Output Connectors	2 BNC connectors
Analog Mux Bandwidth	250 MHz (typical)
Analog Mux Attenuation	10:1 (typical)

Power Requirements

Power Line Voltage	90 V AC to 250 V AC
Power Line Frequency	45 Hz to 66 Hz
Maximum Power Consumption	325 W

TECHNOLOGY

Logic Analyzer

APPLICATIONS

High-Speed Digital System Debugging, Bus Analysis, and Timing Verification