

TEKTRONIX

TLA5204B

The Tektronix TLA5204B is a 136-channel logic analyzer from the TLA5000B Series designed for digital designers debugging single-bus timing and state operations. It features 125 ps MagniVu high-speed timing acquisition simultaneously with conventional timing and state analysis, up to 32 Mb record length, 235 MHz state acquisition, and integrated iView digital-analog cross-domain analysis on a Windows XP Professional controller.

SPECIFICATIONS

General

Display	10.4-inch active-matrix color TFT LCD, 1024 × 768 XGA resolution
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General System Architecture

Total Logic Channels	136 (128 data channels, 8 clock channels)
MagniVu Timing Memory Depth	16 Kb per channel

Timing Acquisition

Max Conventional Timing Sample Rate	2.0 GHz (500 ps) half-channel / 1.0 GHz (1 ns) full-channel
Max MagniVu Timing Sample Rate	8.0 GHz (125 ps)
MagniVu Timing Resolution	125 ps

State Acquisition

Max State Clock Rate	235 MHz
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Triggering and Event Recognition

Trigger Sequences	16 sequence states
Word Recognizers	16 word recognizers
Range Recognizers	4 range recognizers

Integrated Host PC Specifications

Internal Operating System	Microsoft Windows XP Professional
Display Type	10.4-inch active-matrix color LCD
Display Resolution	1024 × 768 pixels (XGA)

Software & Protocol Analysis

Oscilloscope Integration	Tektronix iView time-correlated digital-analog waveform display
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Interfaces & Connectivity

USB Ports	USB 2.0 ports
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TECHNOLOGY

Logic Analysis

APPLICATIONS

Digital System Debug, Embedded Hardware Validation, State and Timing Analysis, Signal Integrity Troubleshooting

Generated by SpecAtlasHub (specatlashub.com). Specifications are compiled from available sources and are subject to change — verify critical values against the manufacturer before purchase.