TEKTRONIX

TLA7AA1

The Tektronix TLA7AA1 is a 34-channel logic analyzer module for the TLA700 and TLA7000 series mainframes. Featuring 32 data channels and 2 clock/qualifier channels, the module utilizes Tektronix's MagniVu™ technology to deliver up to 8 GHz (125 ps) high-resolution timing analysis alongside simultaneous state analysis up to 800 MHz. Designed for debugging complex digital systems, it supports advanced triggering, transitional storage, and low-loading compression probing.

SPECIFICATIONS

General

Interfaces	Mainframe backplane, Tektronix compression probe interface
Warm-up Time	30 minutes
Recommended Calibration Interval	1 year

Physical

Power Supply	Powered by mainframe slot; Power dissipation: 75 W (typical), 100 W (maximum)
Operating Temperature	0 °C to +50 °C °C
Dimensions (W×H×D)	59 mm × 262 mm × 373 mm mm
Weight	2.1 kg

Channel and Acquisition Performance

Number of Channels	34 (32 data, 2 clock/qualifier)
Data Channels	32
Clock/Qualifying Channels	2
Maximum State Acquisition Speed	Up to 800 MHz (option dependent: 120 / 200 / 450 / 800 MHz)
Maximum Conventional Timing Speed (Half Channel)	2.0 GHz (500 ps)
Maximum Conventional Timing Speed (Full Channel)	1.0 GHz (1 ns)
Maximum MagniVu Timing Speed	8.0 GHz (125 ps)
MagniVu Timing Resolution	125 ps
MagniVu Memory Depth	16 kb per channel
Acquisition Memory Depth (Half Channel)	Up to 64 Mb (option dependent: 128 kb, 512 kb, 2 Mb, 8 Mb, 16 Mb, 32 Mb, 64 Mb)
Acquisition Memory Depth (Full Channel)	Up to 32 Mb (option dependent: 64 kb, 256 kb, 1 Mb, 4 Mb, 8 Mb, 16 Mb, 32 Mb)
Setup and Hold Window	1.0 ns
Minimum Pulse Width (Conventional)	1.25 ns
Minimum Pulse Width (MagniVu)	250 ps
Transitional Storage	Supported

Triggering and Sequencing

Number of Trigger States	16
Word Recognizers	16 (34 bits wide)
Range Recognizers	4 (34 bits wide)
Transition Detectors	4 (34 bits wide)
Counter/Timers	2 (16-bit counters or 51-bit timers)
Trigger Position	Pre-trigger, post-trigger, or delay
Glitch/Violation Triggering	Yes (1.25 ns minimum pulse width)
Setup and Hold Violation Triggering	Yes
Multi-Module Trigger Linkage	Supported via mainframe trigger bus

Analog Properties & Probe Interface

Input Impedance (Resistance)	20 kΩ (with P68xx/P69xx probes)
Threshold Voltage Range	-2.0 V to +4.5 V
Threshold Setting Resolution	10 mV
Threshold Voltage Accuracy	±(35 mV + 1% of setting)
Maximum Input Voltage (Absolute)	±15 V
Supported Probe Families	P6800 series, P6900 series
Probe Connection Type	Low-loading compression probing system
Analog Output / Mux	Supported (routes any digital channel to analog output SMB)

Clocking and Timing Modes

Clocking Modes	State, Conventional Timing, MagniVu Timing, Transitional
Clock Qualifiers	4
Clock Demultiplexing Modes	1:2, 2:1, Demux-H, Demux-L

Mainframe Compatibility & Host Interface

Compatible Mainframes	TLA7000 Series (TLA7012, TLA7016), TLA700 Series (TLA714, TLA715, TLA721)
Module Slot Width	2 slots
Required Controller Software	TLA Application Software V4.1 or higher
Oscilloscope Integration	iView™ (external Tektronix oscilloscope integration supported)

Environmental & Safety Compliance

Storage Temperature Range	-20 °C to +60 °C
Relative Humidity (Operating)	20% to 80% RH (non-condensing)
Relative Humidity (Non-operating)	5% to 90% RH (non-condensing)
Maximum Operating Altitude	3,000 m (10,000 ft)
Maximum Non-operating Altitude	12,190 m (40,000 ft)

Electrical

Minimum Input Voltage Swing	300 mV p-p (single-ended), 150 mV p-p (differential)

Analog Mux

Analog Multiplexer Bandwidth	3 GHz (with P69xx probes), 2 GHz (with P68xx probes)

Environmental

Operating Shock	30 g (11 ms, half-sine)
Non-operating Shock	50 g (11 ms, half-sine)
Operating Vibration	0.31 g RMS (5 Hz to 500 Hz)
Non-operating Vibration	2.46 g RMS (5 Hz to 500 Hz)

Analog Output / Mux

Analog Output Connector	SMB

TECHNOLOGY

Logic Analyzer Module

APPLICATIONS

Digital system debugging, hardware verification, FPGA debug, and high-speed timing analysis