TEKTRONIX

TLA7AA2

The Tektronix TLA7AA2 is a high-performance 68-channel logic analyzer module for the TLA7000 and TLA700 series mainframes. Designed for synchronous state and high-speed asynchronous timing analysis, it offers simultaneous state, high-speed timing, and analog analysis through a single probe pin. The module features Tektronix's proprietary MagniVu acquisition technology, delivering up to 125 ps (8 GHz) timing resolution alongside deep memory timing analysis.

SPECIFICATIONS

General

Display	None (Mainframe dependent)

Physical

Power Supply	Mainframe dependent
Dimensions (W×H×D)	1-slot wide TLA module mm

Channel and Input Characteristics

Number of Channels	68 (64 data, 4 clock)
Input Impedance	20 kΩ
Minimum Input Voltage Swing	300 mV
Threshold Voltage Range	-2.0 V to +4.5 V
Threshold Accuracy	±(35 mV + 1% of setting)
Threshold Resolution	10 mV

Timing Acquisition (Asynchronous Mode)

MagniVu Timing Sample Rate	8 GHz (all channels)
MagniVu Timing Resolution	125 ps (all channels)
Maximum Timing Sample Rate (Half Channel)	2.0 GHz (500 ps)
Maximum Timing Sample Rate (Full Channel)	1.0 GHz (1.0 ns)

State Acquisition (Synchronous Mode)

Maximum State Clock Rate	135 MHz (with Option 1S) / 235 MHz (with Option 2S) / 450 MHz (with Option 3S)
Maximum State Data Rate	135 Mb/s (with Option 1S) / 235 Mb/s (with Option 2S) / 450 Mb/s (with Option 3S)
Number of State Clocks	4

Memory and Record Length

MagniVu Memory Depth	16 Kb per channel
Acquisition Timestamp Resolution	125 ps

Triggering System

Number of Trigger States	16
Word Recognizers	16
Range Recognizers	4
Glitch Recognizers	Yes (on all channels)
Setup/Hold Violation Recognizers	Yes (on all channels)
Trigger Counters/Timers	2 counters, 2 timers

Probing Options and Connectivity

Compatible Probes	P6800 series (including P6810, P6860, P6880)

Mainframe Compatibility and Integration

Compatible Mainframes	TLA7012, TLA7016, TLA715, TLA721, TLA7XM
Number of Slots Required	1

Performance Options

State Speed Options	135 MHz (Opt. 1S) / 235 MHz (Opt. 2S) / 450 MHz (Opt. 3S)
Memory Depth Options	512 Kb (Opt. 1M) / 2 Mb (Opt. 2M) / 8 Mb (Opt. 3M) / 32 Mb (Opt. 4M)

Inputs & Outputs

Probe Connectors	2 (high-density)

Environmental

Non-operating Temperature	-20 °C to +60 °C
Operating Altitude	3,000 m (9,843 ft)
Non-operating Altitude	12,192 m (40,000 ft)
Operating Shock	30 g (11 ms half-sine)
Non-operating Shock	50 g (11 ms half-sine)
Operating Vibration	0.31 g RMS (5 to 500 Hz)
Non-operating Vibration	2.46 g RMS (5 to 500 Hz)

Compliance

Safety Certifications	UL 3111-1, CAN/CSA C22.2 No. 1010.1, EN 61010-1
Electromagnetic Compatibility	EN 61326, FCC Part 15 Class A

Analog Multiplexer (iView)

Analog Outputs	4 channels, routed to front-panel SMB connectors
Analog Out Bandwidth	2 GHz (typical)
Analog Out Rise Time	250 ps (typical)
Analog Out Signal Delay	6.0 ns (typical)
Analog Out Channel-to-Channel Skew	100 ps (typical)

Power Requirements

+5 V Current Draw	1.5 A
-5.2 V Current Draw	12.8 A
-2.0 V Current Draw	3.4 A
+12 V Current Draw	0.7 A
+3.3 V Current Draw	0.1 A
Power Dissipation	91 W

Software & Compatibility

Minimum Software Version	TLA Application Software V4.1

Acquisition System

Number of Clock Qualifiers	4

TECHNOLOGY

Logic Analysis

APPLICATIONS

High-speed digital system debugging, bus analysis, and hardware-software integration

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