TEKTRONIX

TLA7BB4

The Tektronix TLA7BB4 is a high-performance 136-channel logic analyzer module designed for the TLA7000 series mainframes. It offers industry-leading MagniVu™ acquisition technology providing up to 20 ps (50 GHz) timing resolution alongside deep memory timing analysis up to 156 ps (6.4 GHz) and state acquisition up to 1.4 GHz clock rate. Compatible with P6800 and P6900 series probes, it enables simultaneous state, high-speed timing, and analog analysis through a single probe pin, making it an invaluable tool for debugging complex digital and embedded systems.

SPECIFICATIONS

General

Interfaces	TLA7000 mainframe backplane interface (PCI Express)
Display	None (headless module, uses host mainframe display)

Physical

Power Supply	Powered by TLA7000 mainframe backplane
Operating Temperature	5 °C to 50 °C °C
Dimensions (W×H×D)	25 mm × 262 mm × 373 mm mm
Weight	1.6 kg kg

General Specifications & Compatibility

Module Type	Logic Analyzer Module
Form Factor	Single-wide TLA7000 module
Host Mainframe Compatibility	TLA7012, TLA7016
Required Slot Count	1 slot
Interface Bus Type	PCI Express (internal backplane)
Hot-Swappable Support	No

Channel & Signal Input Characteristics

Total Input Channels	136
Dedicated Clock Channels	4
Dedicated Qualifier Channels	4
Input Impedance (Resistance)	20 kΩ (probe dependent, e.g., P6800/P6900)
Input Impedance (Capacitance)	Down to 0.5 pF (probe dependent)
Threshold Voltage Range	-2.0 V to +4.5 V
Threshold Setting Resolution	5 mV
Threshold Setting Accuracy	±(35 mV + 1% of setting)
Threshold Presets	TTL, CMOS, ECL, PECL, LVPECL, LVCMOS, GTL, SSTL, HSTL
Input Dynamic Range	5.5 V p-p
Maximum Input Voltage (Non-Destructive)	±15 V
Compatible Probe Types	P6800 Series, P6900 Series

Logic Acquisition & Timing Performance

Maximum State Clock Rate	Up to 1.4 GHz (configuration dependent)
Maximum State Data Rate	Up to 3.0 Gb/s (configuration dependent)
MagniVu Timing Resolution	20 ps (50 GHz)
MagniVu Sample Window Size	20 ns (per channel)
Deep Memory Timing Resolution (Full-Channel)	Up to 625 ps (1.6 GHz)
Deep Memory Timing Resolution (Half-Channel)	Up to 312.5 ps (3.2 GHz)
Deep Memory Timing Resolution (Quarter-Channel)	Up to 156 ps (6.4 GHz)
Minimum Detectable Pulse Width	200 ps
Setup and Hold Time Range	-13.0 ns to +17.0 ns
Setup and Hold Window Resolution	80 ps
Channel-to-Channel Skew	Typically <100 ps
Acquisition Memory Depth Options	2 Mb, 4 Mb, 8 Mb, 16 Mb, 32 Mb, 64 Mb
Transitional Timing Resolution	Up to 625 ps (1.6 GHz)
Independent Clocking Support	Yes
State Valid Window	180 ps

Triggering & Sequence Control

Number of Trigger Sequence States	16 states
Trigger State Transition Conditions	16 per state
Word Recognizers	16
Range Recognizers	4
Edge/Transition Recognizers	4
Event Counters	Two 32-bit counters
Time Counter Resolution	50.1 ps
Trigger Actions	Trigger, Trigger All, Store, Don't Store, Start Timer, Stop Timer, Reset Timer, Increment Counter, Decrement Counter, Signal Out
External Trigger Input to Output Latency	Typically <55 ns
Pattern Recognizers	16
Timer Range	Up to 4.5 days
Timer Resolution	50.1 ps

Application-Specific & Extension Functions

Simultaneous State and Timing	Yes (through same probe pin)
Simultaneous Analog Analysis	Yes (via iView and compatible oscilloscope)
Software Execution Tracing	Yes (real-time, nonintrusive, correlated to source code)
Upgrade Path	PowerFlex upgradeable (state speed and memory depth)

Physical, Power & Environmental

Storage Temperature	-20 °C to +60 °C
Operating Humidity	20% to 80% RH (non-condensing)
Storage Humidity	5% to 90% RH (non-condensing)
Operating Altitude	Up to 3,000 m (9,843 ft)
Non-Operating Altitude	Up to 12,192 m (40,000 ft)
Power Dissipation	Typical 85 W (maximum 125 W)
Coolant Type	Forced air (from mainframe fans)

Compliance, Calibration & Standards

Calibration Cycle	1 year
Standard Warranty	1 year
Safety Certifications	UL61010-1, CAN/CSA-C22.2 No. 61010-1, EN61010-1
EMC Compliance	EU EMC Directive, FCC Part 15 Class A, AS/NZS CISPR 11

Performance

State Speed Options	450 MHz (Opt. 1S) / 900 MHz (Opt. 2S) / 1.4 GHz (Opt. 3S)
Memory Depth Options	2 Mb (Opt. 1M) / 8 Mb (Opt. 2M) / 32 Mb (Opt. 3M) / 64 Mb (Opt. 4M)
Minimum Eye Width	300 ps
Minimum Eye Height	150 mV (single-ended), 100 mV (differential)
Maximum Merged Channels	680 channels (up to 5 modules)
Demultiplexing Support	Yes, 2X and 4X modes
Minimum Setup/Hold Window	180 ps (3.0 Gbps data rate, setup + hold)

Inputs & Outputs

iView Port Connector	SMB female
Probe Connectors	4
Channels per Probe Connector	34 (32 data channels, 2 clock/qualifier channels)

Triggering

Trigger Sequence Rate	500 MHz (2 ns)
Number of Timers	2
Maximum Counter Frequency	500 MHz
Trigger Position Accuracy	±1 sample clock period
Storage Qualification	By state, by sequence state, or by word

Software & Control

Required Software Version	TLA Application Software Version 5.1 or higher

TECHNOLOGY

Logic Analyzer Module

APPLICATIONS

High-speed digital system debugging, hardware/software integration, and embedded system validation