TEKTRONIX

TLA7N1

The Tektronix TLA7N1 is a 34-channel logic analyzer module designed for the TLA700 series mainframes. It provides high-performance state and timing analysis, featuring Tektronix's proprietary MagniVu technology for high-resolution timing measurements simultaneously with deep timing and state acquisitions.

SPECIFICATIONS

General

Interfaces	Via TLA700 series mainframe backplane (probe connections on front panel)
Display	None (uses the host mainframe display)

Physical

Power Supply	Powered via host mainframe backplane slot
Operating Temperature	0 °C to +50 °C °C
Dimensions (W×H×D)	30.5 × 262 × 373 mm mm

System & Chassis Architecture

Number of Channels	34 channels (32 data, 2 clock/qualifier)
Module Slot Width	1 slot (single-wide TLA700 series module)
Mainframe Compatibility	TLA700 Series Mainframes (including TLA714, TLA715, TLA720, TLA721, TLA7012, TLA7016)
Module Merging	Up to 5 modules can be merged to expand channel count (mainframe slot dependent)

RF, Electrical & Calibration Performance

State Speed Options	100 MHz (Option 1S), 200 MHz (Option 2S), 235 MHz (Option 3S), 450 MHz (Option 4S), 800 MHz (Option 5S)
Memory Depth Options	512K, 2M, 8M, or 32M samples per channel (upgrade option dependent)
Input Voltage Range	-2.0 V to +4.5 V
Supported Threshold Presets	TTL, CMOS, ECL, PECL, LVPECL, GTL, GTL+, SSTL, SSTL3, HSTL, User-defined
Input Impedance	20 kΩ (probe dependent)
Compatible Probes	P6417, P6418, P6434 high-density logic analyzer probes

Timing & Synchronization

MagniVu Timing Resolution	125 ps (8 GHz) acquisition simultaneous with deep timing/state on all channels
MagniVu Memory Depth	16 Kb per channel
Deep Timing Resolution (Full Channel)	4 ns (250 MHz)
Deep Timing Resolution (Half Channel)	2 ns (500 MHz)
Trigger State Machine States	16
Word Recognizers	16
Range Recognizers	4
Transition Recognizers	4
Counters/Timers	2 (32-bit)
Glitch/Setup & Hold Triggering	Yes (on any channel)

Environmental Specifications

Storage Temperature Range	-55 °C to +75 °C
Operating Humidity Range	20% to 80% relative humidity, non-condensing

Compliance & Certifications

Product Safety Certifications	UL3111-1, CSA C22.2 No. 1010.1, EN61010-1
Electromagnetic Compatibility Standards	EN61326, FCC Class A, VCCI Class A

Channel Characteristics

Number of Clock Channels	2

Thresholds

Threshold Accuracy	±(35 mV + 1% of setting)

Triggering

Minimum Glitch Width	1.25 ns

Channel Configuration

Data Channels	32

Acquisition System

Acquisition Modes	State, Timing, MagniVu

Trigger System

Trigger Position	Anywhere in memory
Trigger Actions	Trigger, Trigger Out, Store, Don't Store, Start Timer, Stop Timer, Reset Timer, Increment Counter, Decrement Counter, Signaller

Physical / Interconnect

Probe Connection Type	100-pin high-density connector

TECHNOLOGY

Logic Analysis

APPLICATIONS

Digital system debug, timing analysis, and state analysis