TEKTRONIX

TLA7PG2

The Tektronix TLA7PG2 is a 64-channel pattern generator module designed for TLA700 and TLA7000 series logic analyzer mainframes. It supports clock rates up to 268 MHz and a standard vector depth of 2 Mb per channel. This module enables flexible stimulations, pattern sequencing, and functional verification across multiple logic families through a variety of compatible external probes.

SPECIFICATIONS

General

Interfaces	Proprietary mainframe backplane interface (external interfaces such as GPIB, LAN, and USB are mainframe-dependent)
Display	None (uses TLA mainframe display)

Physical

Power Supply	Powered by TLA700/TLA7000 series mainframe backplane
Operating Temperature	5 °C to +50 °C °C
Dimensions (W×H×D)	54 mm × 262 mm × 373 mm mm
Weight	2.3 kg kg
Mainframe Slot Occupancy	2 slots (double-wide)

Channel Configuration

Number of Channels	64 data channels, 4 clock/strobe channels (1 per 16-channel probe)

Timing and Frequency

Maximum Clock Rate (Full-Channel Mode)	134 MHz (64 channels active)
Maximum Clock Rate (Half-Channel Mode)	268 MHz (32 channels active)
Maximum Data Rate (Full-Channel Mode)	134 Mb/s
Maximum Data Rate (Half-Channel Mode)	268 Mb/s
Internal Clock Range	10 Hz to 268 MHz
Internal Clock Frequency Resolution	4 digits
External Clock Input Frequency Range	DC to 268 MHz

Memory and Sequencing

Memory Depth (Full-Channel Mode)	2,097,152 (2 Mb) vectors per channel
Memory Depth (Half-Channel Mode)	4,194,304 (4 Mb) vectors per channel
Pattern Sequencing Steps	1 to 1000 steps
Block Loop Count Range	1 to 65,536
Loop Nesting Depth	8 levels
Number of Subroutines	Up to 256
Sequence Control Commands	Go To, Loop, Call, Return, Wait, Halt

Trigger and Clock Interface

External Clock Input Connector	SMB
External Clock Input Impedance	50 Ohm or 1 kOhm
Event Inputs (Internal/External)	4 (Event A, Event B, Event C, Event D)
Event Input Delay to Data Output	15 clock cycles + 35 ns
External Trigger Input Connector	SMB
External Trigger Output Connector	SMB
Inter-Module Triggering	Via TLA Mainframe Backplane (System Trigger)

System Integration

Compatible Mainframes	Tektronix TLA700 series, TLA7000 series
Software Interface	TLA Pattern Generator Application (embedded in TLA System Software)
Vector Import Formats	ASCII, Tektronix HFS, Tektronix DAS, CSV
Programming Command Support	SCPI-like commands via mainframe programmatic interface

Physical and Compliance

Module Form Factor	Double-wide TLA module
Storage Temperature Range	-20 °C to +60 °C
Relative Humidity Range (Operating)	20% to 80% (non-condensing)
Operating Altitude Limit	Up to 3,000 m (10,000 ft)
Electromagnetic Compatibility (EMC)	EN61326-1 Class A, FCC Part 15 Class A

Probe Compatibility

Supported Logic Families	TTL, CMOS, ECL, PECL, LVPECL, LVDS, LVCMOS (dependent on external probe used)
Compatible Probes	P6470, P6471, P6472, P6473, P6474, P6475
P6470 Probe Logic Support	TTL / CMOS (5 V, 3.3 V)
P6471 Probe Logic Support	ECL
P6472 Probe Logic Support	PECL / LVPECL
P6473 Probe Logic Support	LVDS
P6474 Probe Logic Support	LVCMOS (1.5 V, 1.8 V, 2.5 V, 3.0 V, 3.3 V)
P6475 Variable Probe Logic Support	Variable levels from 1.5 V to 5.0 V
P6475 Variable Delay Channels	2 channels
P6475 Delay Adjustment Range	0 to 10 ns
P6475 Delay Resolution	20 ps
P6475 High Level Output Range	+1.5 V to +5.0 V
P6475 Low Level Output Range	-2.0 V to +3.5 V (High Level dependent)
Probe Outputs Protection	Short circuit and electrostatic discharge protection

Performance

Maximum Merged Modules	Up to 4 modules (up to 256 channels)

External Clock Input

External Clock Input Minimum Amplitude	400 mV p-p
External Clock Input Minimum Pulse Width	1.8 ns

Event Inputs

External Event Input Impedance	1 kΩ (nominal)
External Event Input Voltage Range	-2.5 V to +5.5 V

Environmental

Operating Vibration	0.31 g RMS (5 Hz to 500 Hz)
Non-operating Vibration	2.46 g RMS (5 Hz to 500 Hz)
Non-operating Shock	294 m/s² (30 g), 11 ms half-sine

Frequency

Internal Clock Period Resolution	10 ps
Internal Clock Frequency Accuracy	±100 ppm

Inputs & Outputs

External Clock Input Threshold Range	-2.5 V to +2.5 V
External Event Input Threshold Range	-2.5 V to +2.5 V
Number of Probe Connectors	4

Power Requirements

Current Draw (+5 V Rail)	3.5 A
Current Draw (-5.2 V Rail)	15.0 A
Current Draw (-2.0 V Rail)	5.5 A
Current Draw (+3.3 V Rail)	1.5 A
Current Draw (+12 V Rail)	0.15 A
Power Consumption	113 W

TECHNOLOGY

Digital Pattern Generation

APPLICATIONS

Digital design verification, logic circuit stimulation, and system-level debugging